Texas Instruments
Hardening Commercial Technologies for Multiple Markets

21st Microelectronics Workshop

James F. Salzman
salzman@ti.com

Distinguished Member Technical Staff
Director of Technology, Radiation Effects
Agenda

• Overview of TI HiRel Technologies & Markets
  – Medical
  – Avionics
  – High Temperature (Down Hole)
  – Automotive/Industrial
  – Space

• Space – The Final Frontier or Deadly Frontier?
  – Semiconductor Radiation Effects

• Enhanced Product Issues and Mitigation Techniques:
  – Total Ionizing Dose (TID)
  – ELDERs
  – Latchup and SEE
  – Extreme Temperature Operation

• Summary
Technology ¥ Product Portfolio

**Technology**

- **Bulk CMOS**
  - (w/ analog & RF capabilities)
  - (180-nm, 45-nm)
  - Digital Design, High Density, High Performance, SRAM, MIM caps, dual Vt transistors, etc.

- **Pure Analog & LinBiCMOS**
  - (0.72-µm, 0.35-µm, 0.25-µm)
  - Mixed-Signal, Power Mosfet Family, cutting edge LDMOS, Digital Libraries, Hi-Speed & Precision

- **RFBiCMOS & RFSiGe**
  - (0.5-µm - 0.35-µm)
  - RF Design, Mature processes

- **BiCOM (BiCMOS)**
  - (RF capabilities)
  - (0.70-µm - 0.35-µm)
  - High Precision High Performance Analog, bonded SOI, deep trench, best BJT’s, etc.

**Applications**

- **Digital Signal Processors (DSP) & Microprocessors, System-On-Chip, Data Converters, DSL product, Logic & Wireless Product**

- **Instrumentation, Signal Conditioning, Motor & Servo Controller, Data Converters, Support Functions BaseBand, Interface Product, Hard Disk Drives (HDD)**

- **Networks, Clock Drivers, Data Transmission Devices, Transceivers, Audio & RF CODEC’s**

- **Medical Devices, Implantable devices, CT Scanner electronics, pace makers, smart pills.**

- **Precision H-S Amplifiers, H-S Data Converter, DSL Line Drivers, Military, Space & Avionic Products, Down Hole & High Temperature Electronics**

---

THE 21st MICROELECTRONICS WORKSHOP
A heritage of manufacturing excellence

- Over 30 Years Commitment to the Military and High Reliability IC Industries
- Broad Expanding Product Spectrum
- Broad Process Capability
- Extended Temperature Range
- Baseline Control
- Enhanced Product Change Notification
- Extended Product Life Cycle (Obsolescence Mitigation)
- Line Restarts

Supported Extended Product Life Cycles
Space Radiation Environment

Protons, Electrons, Heavy Ions

Effects
- Total Ionizing Dose (TID)
- Protons
  - Displacement Damage
  - Total ionizing Dose
- Heavy Ions
  - Single Event Effects – SEE
  - Upset - SEU
  - Latch-up - SEL
  - Burnout – SEB
- Charging
- Neutrons for Terrestrial Environment
  - Displacement Damage
  - SEE
HiRel SPACE Products & Technology

The Future of Space

Space is a Global territory for Semiconductors

Over 50 Commercial Launches each year:
- Imaging, Weather, Communications
- Increase system complexity & Data rates
- Defense related Satellites drive more opportunities

Texas Instruments offers a complete “signal chain” QML-V products line for Space
Semiconductor Ionizing Radiation Effects

Oxide and Interface-Trap Charge Creation In MOS Devices

- e-h pairs created by ionizing radiation
- \( N_{it} \): interface trap formation
- \( N_{ot} \): deep hole trapping (E') near interface
- hopping transport of holes through localized states in bulk SiO2

\( + \) \( + \) \( + \) \( + \)

\( H^+ \) proton transport

\( + \) \( + \) \( + \) \( + \)

Gate voltage

PMOS

Drain current

NMOS

PMOS: P-channel Metal-Oxide-Semiconductor Field-Effect Transistor

NMOS: N-channel Metal-Oxide-Semiconductor Field-Effect Transistor
Photoemission NMOS Test

Photoemission Bias Conditions: 0V Gate, Source and Substrate, 5V Drain

NMOS Test Structure Pre Rad
Ids = 0uA

NMOS Test Structure 10K Rad
Ids = 7uA

NMOS Test Structure
Impact of Total Dose on MOS Structures

Radiation-induced charging (usually positive) of dielectrics leads to the turn-on of parasitic oxide transistor compromising well isolation. (In submicron technologies the gate oxides are so thin that intrinsic total dose effects are minimal)

TID Improvement Techniques

- Thin Gate Oxide
- Slow Gate Growth
- Limit Hydrogen in process
- Limit Implant Damage
  - Thicker Poly
  - Pre implant Gate Ox
- Optimize Vt’s
- Hardened Oxide
- Channel Stop
- Enclosed Gate
- Guard Rings
- LOCOS v.s. STI
Hardened CMOS Logic Families

TI is hardening its AC and HC Logic Family Lines

Edge Leakage: due to charge trapping in region of transition from gate oxide to field oxide – Bird’s beak region formed by LOCOS process.

(from course on Radiation Effects, 2006, Martin Dentan)
Additional Birds Beak Reticle Generated using WPG Extracts & CS Implant

Boron Implant into BB area around NFETS Only

15K rad performance ➔ improved to 50K rads

VTN BB 1E13
C/S 1E14

0k
50k
100k

-0.50 0.50 1.50 2.50 3.50
Vgs (V)

Ids (A )

0k
50k
100k

-0.50 0.50 1.50 2.50 3.50
Vgs (V)
Under high dose rate there is a high generation of electron-hole pairs (charge yield). The holes are forced to the interface by positive gate voltage, while the electrons are swept away into the gate. The buildup of holes at the interface form a positive charge barrier and repel the generated protons (hydrogen), keeping them from the interface and forming interface states. They typically will recombine.

Under lose dose rates there is low generation of electron-hole pairs. The holes are forced to the interface by positive gate voltage, while the electrons are swept away, in the same way under high dose rate, but the trapped hold buildup is much lower. The repelling force of the trapped holes is low enough to allow the generated protons (hydrogen) to migrate to the interface forming interface states.
The Effects of Hydrogen in IC Processing

Test transistors and circuits subjected to small amounts of hydrogen trapped in hermetically sealed packages can significantly degrade the total dose and dose rate response of bipolar linear microelectronics.

Ronald L. Pease
IEEE Transactions on Nuclear Science, December 2004
ELDRS Unitrode & Swift Product Hardening
( New Releases > 30Krad )

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>0.8V</th>
<th>0.9V</th>
<th>1.8V</th>
<th>2.5V</th>
<th>2.7V</th>
<th>3.3V</th>
<th>5V</th>
<th>5.5V</th>
<th>6.0V</th>
<th>9.0V</th>
<th>10V</th>
<th>12V</th>
<th>17V</th>
<th>36V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Current</td>
<td>14A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10A</td>
<td></td>
<td></td>
<td></td>
<td>6A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6A</td>
<td></td>
<td></td>
<td></td>
<td>3A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6A</td>
<td></td>
<td></td>
<td></td>
<td>3A</td>
<td></td>
<td></td>
<td></td>
<td>1.5A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.5A</td>
<td></td>
<td></td>
<td>1A</td>
<td></td>
<td></td>
<td></td>
<td>1A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1A</td>
<td></td>
<td>800</td>
<td></td>
<td></td>
<td></td>
<td>600</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>600</td>
<td>300</td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Step down DC/DC Converter (SWIFT)
TPS54xxx

Step down DC/DC Converter
TPS62xxx

Step up DC/DC Converter
TPS61xxx

LDO - Linear Regulators
TPS7xxx

Step up DC/DC Converter (Charge Pumps)
TPS60xxx
REG7xx

THE 21st MICROELECTRONICS WORKSHOP
Japan Aerospace Exploration Agency
Single Event Effects

**SEE**
- Single Event Effects

**SET**
- Single event transient

**SBU**
- Single bit upset

**MBU**
- Multiple bit upset

**SEFI**
- Single event functional interrupt

**SEL**
- Single event latch-up
  - (May Still Function)

**SEGR/SEB**
- Single event gate rupture/Burnout

**SEU**
- Single event upset

**Soft Error**

**Hard Error**

---

THE 21st MICROELECTRONICS WORKSHOP
Buried Layers can reduce Charge Collection
Atmospheric Radiation Effects

GENERATION OF THE ATMOSPHERIC RADIATION ENVIRONMENT

• “Cosmic Rays” interact with the Earth’s atmosphere

• Incoming Radiation
  • Galactic sources
  • Solar Energetic Particles

• Resultant large flux of high energy secondary neutrons

<table>
<thead>
<tr>
<th>Approximate Comparisons</th>
<th>1 - 10 MeV</th>
<th>&gt;10 MeV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground level [Singapore]</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>Altitude 40,000 ft [Singapore]</td>
<td>330</td>
<td>1605</td>
</tr>
<tr>
<td>Ground level [New York]</td>
<td>10</td>
<td>19</td>
</tr>
<tr>
<td>Altitude 40,000 ft [New York]</td>
<td>3100</td>
<td>6000</td>
</tr>
<tr>
<td>Altitude 40,000 ft [Polar]</td>
<td>4536</td>
<td>8779</td>
</tr>
</tbody>
</table>

Production of Secondary Atmospheric Neutrons

IBM Journal of Research and Development, Vol 40
Soft Error Rate (SER) produces the highest failure rate in commercial electronics of all other reliability mechanisms combined.

Many types of Mitigation techniques are used today to improve SER caused from atomic particles.
In the medical arena the focus is on implantable devices. In general the demographic for implantables is the same demographic that will receive radiation treatments. Luckily most radiation treatments are highly focused – for example focused x-ray beam exposures such that the dose to sensitive areas such as implantables can be minimized. For some therapies however, the whole body is exposed to high fluxes of protons and/or neutrons. (Medtronic – Jeff Wilkinson)

Primary Effects

- Total Dose Effects
- Single event effects

More Electronics are now in the Beam (no more film)
Latch-up Effects on ICs

Transient currents induced by ionizing radiation can trigger the parasitic SCR. Latchup requires forward biasing the n+/psub junction, & forward biasing of the p+/nwell junction, and sufficient gain of parasitic bipolar transistors.

If SCR goes into a “latched” state, large amounts of current can flow between Vcc and Vss leading to loss of circuit functionality and in extreme cases melting of bond wires and metal leads.

Equivalent Circuit of parasitic pn-pnSCR

Latch-up occurs when the Hfe product is > 1
A low resistivity starting substrate is used, and then a higher resistance Silicon Epitaxial film (Epi) is grown to enable working CMOS. Parasitic bipolar action between the various junctions is greatly reduced improving tolerance against latch-up.

The approach of using a layer of low resistivity below the CMOS wells to reduce latch-up has been in use for many years.
What is NBTI?

Negative Bias Temperature Instability (NBTI) is a \( I_{dsat} \) issue. There is a \( V_t \) shift observed when \(-V\) bias is applied to the gate of a PMOS transistor (inversion), or, equivalently, when the gate is grounded and a \( V \) bias exists on the S/D and well.

Dramatically effects the operating lifetime of Semiconductors, in simple terms it is a Reliability issue.

\[
\equiv Si-H + A + p^+ \leftrightarrow \equiv Si^+ + B^+
\]

This fits a large portion of the known elements of \( V_{min} \) shifts: sensitivity to hydrogen, bake recovery, saturating behavior, temperature, voltage, and circuit sensitivity.

How do we attack NBTI in the process?

1. Minimize \( T(0) \) interface trap concentration.
   A. Oxide type, growth conditions
   B. Control process damage
2. Minimize presence Hydrogen
3. Minimize hole concentration (lower \( E, V \)).

These techniques can be used to harden against Total Dose
Down Hole Drilling Electronics

- **Environmental Operating Issues**
  - Shock and vibration
  - Temperature and pressure
  - High reliability over target lifetime

Seismic applications
-40° C to +125° C 1 year

Logging while drilling
-40° C to +150° C 1000 hours
-40° C to +175° C 200 hours

Wireline
-40° C to +175° C 400 hours

Reservoir monitoring
+150° C to +225° C 6 months

Permanent applications
+150° C 5 years

Very Critical to minimize NBTI & Leakage!!
Same Techniques are used to harden against Radiation & High Temp
BiCOM-3 Technology Overview

High-Speed & Performance

Technology Features:
- Complementary SiGe BiCMOS
- 0.35 μm Class
- SiGe on SOI
- Triple Metal
- 5V & 3.3V CMOS
- Isolated CMOS
- 5V SiGe NPN
- 5V SiGe PNP
- TFR: NiCrAl 50 Ω/sq
- C: 0.7 fF/um² MIM
- R: Poly 290 Ω/sq
- Bipolar Performance:

<table>
<thead>
<tr>
<th></th>
<th>NPN</th>
<th>PNP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$H_{FE}$</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>$V_A$</td>
<td>150</td>
<td>100</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>7.0</td>
<td>6.0</td>
</tr>
<tr>
<td>$f_T$</td>
<td>18</td>
<td>18</td>
</tr>
</tbody>
</table>

Process Extensions:
- 200mm Wafers
- Status: In Production

- Latch up Free
- TID > 150K Rad(si)
- ELDRS Free
- Easy Photo Compensation

Bipolar Performance:
- HFE 200 100
- $V_A$ 150 100
- $BV_{CEO}$ 7.0 6.0
- $f_T$ 18 18
Total Irradiated Dose is a problem in medical, industrial sterilization, and space based electronics.
- Process techniques can help improve tolerance to TID
- Same techniques are applied to improve reliability (NBTI)
- Same techniques are applied for higher temperature operations for Down Hole Drilling
- Circuit Design techniques can also be used, but this is not the TI approach (point solutions only)

Latch-up is a major issue for all applications. Standard latch-up prevention techniques are used across all technologies at Texas Instruments.
- Buried diffusion and implanted layers, Epi layers, etc.

SEE’s is a dominant failure mode in advanced microelectronics.
- Includes Medical, Avionics, and Space based applications
- Buried diffusion and implanted layers & circuit design techniques are used to mitigate.

TI addresses Global markets, i.e. Medical, Avionics, Down Hole, Space based systems. These are all faced with the same issues: Particles, TID, NBTI, Temperature, etc. TI’s Medical HiRel strategy is to apply global process fixes to address multiple market uses for it’s products.

By Addressing the Global Market, products are offered at lower cost.
Thank You

www.ti.com/space
Fuji Electronics – kotake@fuji-electronics.com
Texas Instruments HiRel Medical Defense and Aerospace organization leverages the large portfolio of TI semiconductor processes to provide HiRel products to the global marketplace. These HiRel applications demand reliable products that must tolerate many types of radiation, high temperature, and extended product life applications. It becomes critical to engage in a business strategy that not only addresses these markets in the United States, but also globally. In many cases by careful planning and execution, global markets can be addressed rather than point solutions. By applying a global mindset to semiconductor processes, entire product families can often become available then to the HiRel marketplace, rather than a single part solution. This presentation will describe global semiconductor process change techniques that can "fix" product families for HiRel applications in the global market place.