Advanced devices with high density technology required for next generation small satellites

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The purpose to development small satellites

Small Satellite provides you with:

- The prompt start up of operation on orbit so as not to miss the best business opportunity,
- Uninterrupted operation on orbit through periodical and successive launches,
- Low cost development process in order to exploit advanced devices,
- Low risk mission deployment through the installation of minimum number of payloads, or often one payload, on one satellite bus exploiting multiple satellites launch chances using piggy-back spaces,
- And more…
Road map of the development of small satellites (1)

- **SDS-1**
- **NEC standard bus (NEXTAR)**
- **SpaceCube 2**
- **ISAS small satellite series**
- **METI advanced small satellite**
- **(300kg~500kg)**

**Development**

- Joint collaboration study with JAXA/ISAS
  - 64bit MPU
  - Burst SRAM
  - SpaceWire

**Standardization**

- **2008 ~ 2009**
- **2011**
- **2013 ~**
Scalable Architecture

- Framework for prompt integration with high reliability
- Applicable for Various kinds of observation mission
- Various figure (topology) for each mission purpose
- Data handling system based on “Scalable” architecture applicable from small satellites up to large satellites is required other than “Fixed common bus”.

Satellite as a composite of function blocks

Satellite constellation

Key components for small satellites

Space Cube 2
- Space Cube architecture based on T-Engine architecture
- SpaceWire interface
- Wide range of compatibility
  - Standard middleware and API (Application Program Interface)
- Small, light weight, low Power Consumption and low cost

Device set
- HR5000/HR5000S
- BSRAM (Burst SRAM)
- POL (Point of Load)
- SpaceWire target interface (NIC: Network interface controller)
- SpaceWire router

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Essential factor realizing small satellites (1)

**High Density FD (Fully Depleted) -SOI ASIC**

- Designed using standard libraries of JAXA authorized CMOS/FD-SOI ASIC
- 0.15 um FD-SOI ASIC

<table>
<thead>
<tr>
<th>Description</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-supply Voltage</td>
<td>Core: 1.5V, I/O: 3.3V</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-45 to 130 degrees C</td>
</tr>
<tr>
<td>No. of Metallization Layers</td>
<td>6 layers</td>
</tr>
<tr>
<td>Target Package</td>
<td>304 pin CQFP, 352 pin CQFP</td>
</tr>
<tr>
<td>Target Chip Size</td>
<td>5mm x 10mm, 10mm x 10mm</td>
</tr>
<tr>
<td>Radiation Resistance</td>
<td></td>
</tr>
<tr>
<td>SEU</td>
<td>LET &gt; 64 [MeV/(mg/cm²)] (target value)</td>
</tr>
<tr>
<td>SEL</td>
<td>SEL Free</td>
</tr>
<tr>
<td>TID</td>
<td>&gt; 1000 [Gy (Si)]</td>
</tr>
</tbody>
</table>
SOI ASIC chip set realizing key components for small satellites

- **NSR14**
  SpaceWire router

- **DFAC**
  GPS receiver correlator

- **HR5000S**
  64bit one-chip micro-controller
Micro Card

- Versatile computer system with name-card size
The policy for using cutting edge devices for small satellites (1)

Basic ideas are that:

- Based on Parts program requirements for science satellite established by ISAS with over 35 years
- Use of Level 2 parts for Non-critical components with project authorization as exception
- Parts Qualification test may be performed according to specification defined by Satellite Manufacturer depending on project requirement
- The project specific advanced parts and cutting edge parts are evaluated with the same methodology for previous science satellites
The policy for using cutting edge devices for small satellites (2)

Definition of Level 2 in EEE-INST-002

- **Level 1:** Parts shall be selected and processed to this level for missions requiring the *highest reliability and lowest level of risk*. Level 1 active parts shall be reviewed for radiation hardness, and radiation testing is required when information is not available. The typical mission duration for Level 1 programs is 5 years or greater.

- **Level 2:** Parts shall be selected and processed to this level for missions with *low to moderate risk*, balanced by cost constraints and mission objectives. Level 2 active parts shall be reviewed for radiation duration for level 2 programs varies from 1 to 5 years.
# Quality level for the parts used for small satellites

## Required Quality Level

<table>
<thead>
<tr>
<th></th>
<th>For Critical Components</th>
<th>For Non-Critical Components</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IC</strong></td>
<td>1) JAXA Qualified or ESCC Level B or MIL Class V or equivalent screened</td>
<td>Same Level for the Parts for Critical Components 1), 2)</td>
</tr>
<tr>
<td></td>
<td>2) MIL QML Q plus PIND</td>
<td>MIL QML Q or equivalent plus PIND</td>
</tr>
<tr>
<td><strong>Transistor Diode</strong></td>
<td>1) JAXA Qualified or ESCC Level B or MIL JANS or equivalent screened</td>
<td>Same Level for the Parts for Critical Components 1), 2)</td>
</tr>
<tr>
<td></td>
<td>2) JANTXV plus PIND</td>
<td></td>
</tr>
<tr>
<td><strong>Resistor, Capacitor, other passive parts</strong></td>
<td>1) JAXA Qualified or ESCC Level C(Level B for Crystal, Fuse, Reference resistor) or MIL ER-R</td>
<td>Same Level for the Parts for Critical Components 1), 2)</td>
</tr>
<tr>
<td></td>
<td>2) Screened with 96h Burn-in</td>
<td></td>
</tr>
<tr>
<td><strong>Hybrid IC</strong></td>
<td>1) JAXA Qualified or MIL QML Class K or equivalent screened</td>
<td>Same Level for the Parts for Critical Components 1), 2)</td>
</tr>
<tr>
<td></td>
<td>2) MIL QML 2) MIL QML Class H plus PIND</td>
<td>MIL QML Class H or equivalent plus PIND</td>
</tr>
<tr>
<td><strong>Connector</strong></td>
<td>1) JAXA Qualified or ESCC Level B or MIL qualified or equivalent screened. Except JAXA or ESA qualified parts, EEE-INST-002 Document Section C2 requirements are added.</td>
<td>Same Level for the Parts for Critical Components 1)</td>
</tr>
</tbody>
</table>
Selection method of advanced devices for small satellites

Test Evaluation item example

- Evaluation for Design Parameters
  - Radiation test
  - Life test
- Structure Analysis
- Failure mode Analysis
- Process and Material Analysis

Use of existing reliability data

Assessment of Manufacturer

- Organization, Quality Management System, Production control, Facility, etc.
Expectation for new device technology required for the new generation of small satellites

**Keywords**

- High density packaging technology and its application technology
  - Smaller Package with small pin count and/or high pin count BGA (Ball Grid Array), CGA (Colum Grid Array)
  - Bare die with high yield

- High-speed transmission technology between substrates
  - Connector, Substrate

- Analog/Mixed-signal IC
High density packaging technology and its application technology required for the new generation of small satellites

QFP to BGA, CGA

- Advanced semiconductors require High pin count Package

Tasks of Process establishment and Inspection method

- To apply BGA and CGA for space components;
  - Surface mount technology with 100% yield, because BGA and CGA can not be re-mounted
  - Micro-focus or CT X-ray inspection, instead of Visual Inspection