Designing A Single Board Computer For Space Using the Most Advanced Processor and Mitigation Technologies

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Maxwell Technologies, Inc.
Overview

- Background
- Maxwell’s Design Strategy
- Maxwell’s Baseline Design
- Upset Mitigation
- Validation and Analysis
Traditional SBC Methods For Space

- Rad-Hard Components

- Commercial Components with Basic Correction
Rad-Hard vs. Commercial MIPS

Performance (MIPS)

Year Introduced

>10 years

Commercial

PPC750GX

PPC750FX

PPC750

PPC603

80486

Rad-Hard

Commercial

PPC603

PPC750FX

PPC750GX

80486
Processor Bits Increasing Exponentially

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Rad-Hard Upset Trend: Less SEU immunity

* Assumes 1E-10 Upsets/Bit-day

Ultracapacitors • Microelectronics • High-Voltage Capacitors
• Rad-Hard Components
  • Typically Lag Commercial Market by 5 to 10 years
  • Lower Performance, Good Upset Rate Per Bit
  • Upset Rate Per Device Is Getting Worse Due to Increased Bits

• Commercial Components with Basic Correction
  • Great Performance, Poor SEU immunity
  • Low Cost, for Non-mission Critical Applications
  • Plastic Parts, Low Screening Levels
Combination of Rad-Hard Components and Architecture Hardened Commercial Technology

- Rad-Hard Parts Where Plausible
- State of the Art Commercial Components In Key Areas
- Flight Boards All Class “S” or Equivalent
- Highest Performance and Best Upset Rates Available
SCS750 Design Strategy

**Commercial Technology**
- Latest SOI PowerPC @ 800MHz
- High Performance SDRAM
- On-Board Control Logic

**Mitigation Technique**
- TMR/Resynch & Scrubbing
- Double Device Correct & HW Scrub (Reed-Solomon)
- Actel RT-AXS Built-in TMR

**Result**
- SCS750
  - 1 Uncorrected Error > 300 Years
  - Better Upset Rate Than Rad-Hard SBC’s!

~ 1 Upset Per Day
Functional Block Diagram

- Actel Rad-Tolerant FPGA
  - SEU Immune
- Reed Solomon And ECC
  - SDRAM 256 Mbytes
  - EEPROM 8 Mbytes

System Controller
- Memory Controller, PCI, Timers, Interrupts, DMA, UART

Triple Modular Redundancy

PowerPC IBM 750FX™
- TMR Protected

PMC #1
- Engineering Development Use Only

PMC #2

PCI-IF
- USRTS, Parallel Ports 1553 Interface

MIL-STD-1553 BC/RT/MT
- SEU Immune

Actel Rad-Tolerant FPGA
- SEU Immune

PCI – PCI Bridge

32 Bit, 33 MHz, cPCI

- Actel Rad-Tolerant FPGA
- SEU Immune
SCS750A Prototype Module

- EDAC Protected EEPROM
- Reed-Solomon Protected SDRAM
- RT FPGA With System Controller, TMR and EDAC
- TMR Protected PPC750FX
- cPCI Connector
- RT FPGA With PCI-PCI Bridge
PPC750FX™ Features

• 0.13um SOI, Copper Interconnect, SiLK
• Extremely Low Power, Runs at 1.2V – 1.5V
• 400MHz ➔ > 900 MIPS
• 800MHz ➔ > 1,800 MIPS
• L1 cache 32KB I, 32KB D with Parity
• L2 Cache 512KByte On-Chip, Built-In SEC/DED
  • L2 Cache Runs at Full Processor Clock Rate
  • Tags Are Parity Protected
Processor Power v. Performance

Performance (MIPS)

Power Consumption - Watts

- Rad-Hard
- SCS750

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The Importance of On Board L2 Cache

![Graph showing the comparison between Maxwell TMR PPC w/L1 & L2 Cache and Rad-Hard PowerPC w/L1 Cache Only.

- Maxwell TMR PPC w/L1 & L2 Cache:
  - Code/Data Size (KBytes): 0 to 350
  - MIPS: 0 to 2000
  - Performance Improvement: 8X

- Rad-Hard PowerPC w/L1 Cache Only:
  - Code/Data Size (KBytes): 0 to 350
  - MIPS: 0 to 350
  - Performance Improvement: 1000X

- Graph highlights the benefits of having an on-board L2 cache in terms of increased MIPS and reduced code/data size.]
Processor Error Correction

- TMR Voting
- SEU Immune
- Error Detection
- Resynch/Scrubbing
Processor Error Correction Sequence

“All Outputs are Voted Every Cycle“

PowerPC IBM 750FX™
PowerPC IBM 750FX™
PowerPC IBM 750FX™

System Controller
Memory Controller, PCI, Timers, Interrupts, DMA, UART

SDRAM
256 Mbytes

EEPROM
8 Mbytes

PCI-IF
USRTS, Parallel Ports 1553 Interface

MIL-STD-1553 BC/RT/MT
SEU Immune

PCI – PCI Bridge

PMC #1
PMC #2

Engineering Development
Use Only

Actel Rad-Tolerant FPGA
SEU Immune

32 Bit, 33 MHz, cPCI
Processor Error Correction Sequence

- PowerPC IBM 750FX™
- PowerPC IBM 750FX™
- PowerPC IBM 750FX™
- System Controller
  - Memory Controller, PCI, Timers, Interrupts, DMA, UART
  - TMR Protected
  - Reed Solomon and ECC

“Majority Vote is Output”

- SDRAM 256 Mbytes
- EEPROM 8 Mbytes
- PCI-IF
  - USRTS, Parallel Ports, 1553 Interface
- MIL-STD-1553 BC/RT/MT
  - SEU Immune
- PCI - PCI Bridge
  - Actel Rad-Tolerant FPGA
  - SEU Immune
- PMC #1
- PMC #2
- Engineering Development
  - Use Only
- 32 Bit, 33 MHz, cPCI

Actel Rad-Tolerant FPGA
SEU Immune

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Processor Error Correction Sequence

“When Outputs Disagree”

- PowerPC IBM 750FX™
- PowerPC IBM 750FX™
- PowerPC IBM 750FX™

System Controller
Memory Controller, PCI, Timers, Interrupts, DMA, UART

- SDRAM 256 Mbytes
- EEPROM 8 Mbytes

PCI-IF
USRTS, Parallel Ports 1553 Interface

MIL-STD-1553 BC/RT/MT
SEU Immune

PMC #1
PMC #2

PCI – PCI Bridge
32 Bit, 33 MHz, cPCI

Actel Rad-Tolerant FPGA
SEU Immune

Engineering Development
Use Only

Actel Rad-Tolerant FPGA
SEU Immune

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Processor Error Correction Sequence

“Bad Processor Is Isolated and Held in Reset”

“Majority Vote is Output with no Delay”

PowerPC IBM 750FX™

PowerPC IBM 750FX™

PowerPC IBM 750FX™

“Majority Vote is Output with no Delay”

SDRAM 256 Mbytes

EEPROM 8 Mbytes

PowerPC IBM 750FX™

PCI – PCI Bridge

Actel Rad-Tolerant FPGA

SEU Immune

System Controller

Memory Controller, PCI, Timers, Interrupts, DMA, UART

EMPROM 8 Mbytes

SDRAM 256 Mbytes

PowerPC IBM 750FX™

PowerPC IBM 750FX™

PowerPC IBM 750FX™

“Bad Processor Is Isolated and Held in Reset”

“Majority Vote is Output with no Delay”

32 Bit, 33 MHz, cPCI

PCI-IF

USRTS, Parallel Ports 1553 Interface

MIL-STD-1553 BC/RT/MT

SEU Immune

Actel Rad-Tolerant FPGA

SEU Immune

Engineering Development Use Only

PMC #1

PMC #2

Actel Rad-Tolerant FPGA

SEU Immune

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During SCRUB Processor State is Flushed to RSP Memory

- PowerPC IBM 750FX™
- PowerPC IBM 750FX™
- PowerPC IBM 750FX™

- Triple Modular Redundancy

- System Controller
  - Memory Controller, PCI, Timers, Interrupts, DMA, UART

- Processor State
  - SDRAM 256 Mbytes
  - EEPROM 8 Mbytes

- PCI – PCI Bridge

- MIL-STD-1553 BC/RT/MT
  - SEU Immune

- PMC #1
  - PMC #2

- Engineering Development Use Only

- Actel Rad-Tolerant FPGA SEU Immune

- Actel Rad-Tolerant FPGA SEU Immune

- PCI-IF
  - USRTS, Parallel Ports 1553 Interface

- 32 Bit, 33 MHz, cPCI

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Processor Error Correction Sequence

“All Processors are RESET

PowerPC IBM 750FX™

PowerPC IBM 750FX™

PowerPC IBM 750FX™

Triplet Modular Redundancy

System Controller
Memory Controller, PCI, Timers, Interrupts, DMA, UART

1

SDRAM
256 Mbytes

EEPROM
8 Mbytes

PMC #1

PMC #2

PCI-IF
USRTS, Parallel Ports 1553 Interface

MIL-STD-1553 BC/RT/MT
SEU Immune

PCI – PCI Bridge

32 Bit, 33 MHz, cPCI

Actel Rad-Tolerant FPGA
SEU Immune

Engineering Development Use Only

0

1

1

1

1

1

1

“Majority Vote is Output with no delay”

“All Processors are RESET” Processor State Is Held in SDRAM
Processor Error Correction Sequence

“Processor State is reloaded and Processing Resumes”

- PowerPC IBM 750FX™
- PowerPC IBM 750FX™
- PowerPC IBM 750FX™

System Controller
- Memory Controller,
- PCI, Timers,
- Interrupts,
- DMA, UART

“Transparent to Application SW”

- SDRAM
  - 256 Mbytes
- EEPROM
  - 8 Mbytes
- PCI – PCI Bridge

Engineering Development Use Only

Actel Rad-Tolerant FPGA
SEU Immune

PCI-IF
- USRTS,
- Parallel Ports
- 1553 Interface

MIL-STD-1553
- BC/RT/MT
SEU Immune

Actel Rad-Tolerant FPGA
SEU Immune
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**Processor Error Correction Flow**

- **Start State**
  - No Errors

  - **User Called Resynch**
  - **Scrub Timer Expired**
    - **Waits for Software Semaphore to Continue**
    - **Resynchronize Processors <1ms delay**

  - **One Processor Error**
    - **Isolate Processor & Flag Error**
      - **Restart 3 Processors & Flag double error**

- **Double Processor Error**

  - Occurs typically once in >12,000 years

  - Software Transparent
    - No Uncorrected Errors
    - Overhead < 0.1%

  - User Called Resynch

  - Scrub Timer Expired

  - One Processor Error
    - Isolate Processor & Flag Error

  - Restart 3 Processors & Flag double error

- **Resynch**
Processor Error Correction

• Triple Modular Redundant (TMR) Processing
  • Three Processors, Each Completely Isolated
  • No Delay in Voting Because All Key Logic Blocks Are on One Chip

• Detection
  • Single Processor Error: Flags and Isolates Processor
  • Detection Of Double Processor Error and Auto Restart

• Resynch/Scrubbing
  • Saves processor States, Resets, Re-Loads Processor States
  • Proven to Correct Any Single Event Effect
  • < 1 Millisecond Delay, < 0.1% Overhead with 1 Second Scrub
  • Timing Is User Controlled
# SDRAM Error Correction Comparison

<table>
<thead>
<tr>
<th>EDAC Description</th>
<th>Data Bits</th>
<th>Check Bits</th>
<th>Correction / Detection Capabilities</th>
<th>Time to First Failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Error Correction</td>
<td>64</td>
<td>0</td>
<td>None</td>
<td>5 days</td>
</tr>
<tr>
<td>Modified Hamming Code 64/8</td>
<td>64</td>
<td>8</td>
<td>SEC, DED</td>
<td>0.5 years</td>
</tr>
<tr>
<td>Triple Modular Redundancy</td>
<td>64</td>
<td>128</td>
<td>SEC, multi-bit errors/device failures</td>
<td>5 years</td>
</tr>
<tr>
<td>Nibble EDAC 64/16</td>
<td>64</td>
<td>16</td>
<td>Nibble Correct, Double Nibble Detect</td>
<td>24 years</td>
</tr>
<tr>
<td>Reed-Solomon</td>
<td>64</td>
<td>32</td>
<td>Double Nibble Correct</td>
<td>12 Million years</td>
</tr>
</tbody>
</table>

Assumptions: 256 Mbyte Memory - Memory Scrub 1 per day
Reed Solomon SDRAM Error Correction

256 Mbytes Useable SDRAM

32 M

8 Devices (Chips)
X 8 X 8 X 8 X 8 X 8 X 8 X 8

Check Bits

4 Devices
X 8 X 8 X 8 X 8

Reed Solomon Corrects Any Double Device Failure

32 M

X 64 bits

X 32 bits
• SDRAM Parallel Reed Solomon Validation
  • VHDL Test Bench Designed to Exercise SDRAM Error Correction Logic
  • VHDL simulation -- Injection of error types:
    • Every Single Bit Error
    • Every Combination of Double Bit Errors
    • Every Single Device Error
    • Every Combination of Double Device Errors

• Processor Error Detection and Correction
  • VHDL Simulations Which Inject Errors in Processors and Validate Detection and Correction
Technology Feasibility Testing

Radiation Test #1 - TAMU

Single Processor Rad Test
- Irradiated One Processor at a Time
- Tested from 1.9 MeV to 92 MeV.
- No Latch Up Detected
- All SEUs In Single Processor Were Corrected
- Predicted Double Error Rate

Radiation Test #2 - TAMU

Triple Processor Rad Test
- Irradiated Three Processor at Once
- Tested at 36 MeV and 77 MeV.
- All SEUs were corrected
- Double Processor Upsets Recovered With Reboot
- Power Cycling Was Never Required
Demonstrated Performance

Processor 2 is Upset
CPU 2 Held in Reset
All three are Resynchronized
Space Processor Radiation Mitigation and Validation Techniques for an 1800 MIPS Processor Board

Heavy Ion Test Results
Gary M. Swift and Farokh Irom
Jet Propulsion Laboratory / California Institute of Technology

Robert Hillman, Mark Conrad and Phil Layton
Maxwell Technologies

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.
SCS750 Triple Processor Results

Reboot rate as a function of upset rate (or flux)

Good correlation with equation
# Error Rate Comparison

<table>
<thead>
<tr>
<th></th>
<th>GCR</th>
<th>DCF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>34 /yr</td>
<td>1.1E-5 /yr*</td>
</tr>
<tr>
<td>GCR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>heavy ions only</td>
<td>250 /flare</td>
<td>0.22 /flare*</td>
</tr>
<tr>
<td>DCF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>including protons</td>
<td>320 /flare</td>
<td>0.36 /flare*</td>
</tr>
</tbody>
</table>

**Notes:** For shielding of 100 mil Aluminum-equivalent, and use of 100% of registers and L1 caches

**GCR** = Galactic Cosmic Ray background at solar minimum

**DCF** = JPL Design Case Flare (at one A.U.)

(similar in size to Oct. ’89 and Jan. ’72 events)

* Scrub @ 10/sec, performance overhead of < 3%
### Error Rate Comparison

<table>
<thead>
<tr>
<th></th>
<th>GCR</th>
<th>DCF heavy ions only</th>
<th>DCF including protons</th>
</tr>
</thead>
<tbody>
<tr>
<td>GCR</td>
<td>0.2 /yr</td>
<td>1.1E-5 /yr*</td>
<td>16,000</td>
</tr>
<tr>
<td>DCF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>heavy ions only</td>
<td>0.6 /flare</td>
<td>0.22 /flare*</td>
<td>3</td>
</tr>
<tr>
<td>DCF</td>
<td>3.4 /flare</td>
<td>0.36 /flare*</td>
<td>9</td>
</tr>
</tbody>
</table>

**Notes:** For shielding of 100 mil Aluminum-equivalent, and use of **100%** of registers and L1 caches

- **GCR** = Galactic Cosmic Ray background at solar minimum
- **DCF** = JPL Design Case Flare (at one A.U.)
  - (similar in size to Oct. ’89 and Jan. ’72 events)
- * Scrub @ 10/sec, performance overhead of < 3%
CONCLUSION

- Under heavy-ion irradiation, the SCS750 upset mitigation scheme detected and corrected all single processor errors.
  - This mitigation scheme proved to be very effective for the test programs used which are very processor intensive.
  - The performance hit for periodic re-syncing (scrubbing) is small.
- Upon the coincidence of an upset in two processors, the SCS750 successfully recovered with a reboot and reported the double processor error.
  - Coincident errors should be very rare in space.
  - In-beam coincident errors occurred at the expected rates.
- Power cycling was never required for correction.

Commercial processors hardened with the SCS750 architecture can give upset rates comparable to or better than the RAD6000 in space environments.