Establishment of LSI Production System
Adopting COT for Space Application

Oct. 27th, 2006
Mikihiko URANO
High-Reliability Engineering & Components Corporation
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1. Background

- The number of items of JAXA qualified products has been decreasing in the last 5 years.

Manufacturers require a big effort to maintain production lines because the volume of the products to be shipped is extremely small.

Ref: Database of JAXA Qualified EEE parts and Materials.
1. Background (cont.)

- Customers can produce LSI quickly, simply, and inexpensively.
- Customers can produce LSI using commercial foundries and do not need to have their own production lines of LSI.
- Customers can design the mask layout to fabricate LSI wafers by themselves.
- Design rules of the mask layout can be provided by foundries.
- CAD (computer-aided design) tools can be utilized to generate the mask layout.
- Customers can realize the complex system by using IP (Intellectual Property) on a chip.
2. Feature

- ELSI production system adopting COT (Customer Owned Tooling) for space application are:
  - Cell layouts (F/F, Latch, etc.) in the mask are introduced by HBD (Hardness-by-Design) method against for SEU/SET.
  - Two or more LSIs can be placed on the same mask and fabricated on the wafer (Multi-project-run method).
  - Specialized companies (Foundry, Assembly House and Test Laboratory) handle each step of LSI production process.
  - The quality assurance company integrates specialized companies and assures the quality and the reliability of LSI for space application.

- The wafer banking can supply LSI stably for the long term to customers.
3.1 LSI生产系统的采用COT

- 電路図の生成
- 証明をシミュレーションで行う
- マルチプロジェクト実行方法
- マスクレイアウトをHBDセルを使用して設計する
- 構成用LSIの品質保証

顧客A
顧客B
顧客C

統合者
組立工場
テストライブラリ

- ファウンデリー：ウエハの製造
- アセンブリ：組立
- スクリーニング：選別
- QC I：品質適合性検査

顧客A、顧客B、顧客C、統合者、ファウンデリー、組立工場、テストライブラリとのLSI生産システムの関係
3. Establishment

3.1 LSI production system adopting COT (cont.)

Circuit Design

Using HBD cells, Creating GDS‡

Multiple use of applicable designs

Manufacture Mask

Manufacture Wafer

Assembly

Screening

QCI

Wafer banking

Commercial foundry line

Investigations prior to manufacturing:

Quality management system

Process diagnosis

Optimization of QC I

Group A (Electrical test)

Use of in-process inspection

Group B (Workmanship)

Group C (Life)

Periodical verification by typical sample

Group D (Package)

Group E (TID)
There are two sites of wafer storage facilities in Japan. Two sites reduce risks of wafer damage such as earthquakes, fires, or any other disaster.

<table>
<thead>
<tr>
<th>Site A</th>
<th>Site B</th>
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<tbody>
<tr>
<td>Tsukuba-shi, Ibaraki</td>
<td>Minamata-shi, Kumamoto</td>
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</tbody>
</table>

Atmosphere and temperature:

- **Site A**: 
  - Temperature: 15°C to 35°C
  - Humidity: Dry air

- **Site B**: 
  - Temperature: 15°C to 35°C
  - Humidity: N2 gas

*Note: The table and the map illustrate the conditions and locations of the wafer storage facilities.*
### Establishment

#### 3.2 Wafer banking (cont.)

**Evaluation flow:** Screening, Life Test and DPA

<table>
<thead>
<tr>
<th>Manufacture Wafer</th>
<th>Assembly</th>
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<tbody>
<tr>
<td>Screening</td>
<td></td>
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<tr>
<td>Life Test</td>
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<tr>
<td>Wafer banking</td>
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</tbody>
</table>

**External visual:**

- Low and High temperature
- Room temperature: Interim (post burn-in) electrical parameters
- 125°C, 240 hours: Burn-in test
- Room temperature: Interim (pre burn-in) electrical parameters
- -65°C to +150°C, 10 cycle: Temperature cycling

**Internal visual and mechanical:**

<table>
<thead>
<tr>
<th>DPA</th>
<th>Quantity</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Die shear test</td>
<td>3</td>
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<td></td>
<td>Bond strength test</td>
<td>2</td>
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<tr>
<td></td>
<td>End-point electrical parameters</td>
<td>2</td>
</tr>
</tbody>
</table>

**Steady state life:**

<table>
<thead>
<tr>
<th>DPA</th>
<th>Quantity</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>125°C, 1000 hours</td>
<td>1</td>
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</table>

**End-point electrical parameters:**

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<th>DPA</th>
<th>Conditions</th>
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<tbody>
<tr>
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<td>125°C, 1000 hours</td>
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**DPA:**

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<td>2</td>
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<tr>
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<td>End-point electrical parameters</td>
<td>2</td>
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</table>

**Steady state life:**

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<tr>
<th>DPA</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>125°C, 1000 hours</td>
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4. Results

4.1 LSI production system adopting COT

The "320MIPS 64bit MPU" was developed with the LSI production system adopting COT for space application, and was fully successful in the development test (equivalent to QT) in accordance with JAXA-QTS-2010.

The "320MIPS 64bit MPU" is going to be qualified to JAXA QML products in accordance with JAXA-QTS-2010 by the end of Nov. 2006.

JAXA 2010/10101XZR for Low-power consumption type.
JAXA 2010/10102XZR for High-speed type.
4. Results (cont.)

4.1 LSI production system adopting COT

HBD cells

JAXA/HIREC

MPU core IP

M IPS Technologies

Peripherals IP

Eureka

Whole logic design

and verification

HIREC

Test

(HIREC)

7mm

10mm

Design

(JAXA/HIREC)

Wafer

(Foundry/0.18um CM OS)

Assembly

(Specialized company)

Radiation-shielding package

HIREC

Screening and Qualification test based on JAXA-QTS-2010.

LSI production system adopting COT for 320MIPS 64bit MPU
4. Results (cont.)

4.2 Wafer banking

- First evaluation tests of the wafers prior to the storage were performed on:
  - Wafer A (0.8um, Bulk, CMOS)
  - Wafer B (0.18um, Epi, CMOS)

<table>
<thead>
<tr>
<th>Storage and 1st Evaluation Test on Wafers</th>
<th>Quantity</th>
<th>Started in</th>
<th>Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer A</td>
<td>1 wafer</td>
<td>Feb. 2004</td>
<td></td>
</tr>
<tr>
<td>Wafer B</td>
<td>12 wafers</td>
<td>Jan. 2005</td>
<td></td>
</tr>
<tr>
<td>Mar. 2005</td>
<td></td>
<td></td>
<td>Complete</td>
</tr>
<tr>
<td>20 wafers</td>
<td></td>
<td>Mar. 2005</td>
<td></td>
</tr>
</tbody>
</table>
4. Results (cont.)

4.2 Wafer banking (cont.)

Temperature and Related Humidity data of Site B

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Related Humidity (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>30%RH or less</td>
</tr>
<tr>
<td>20</td>
<td></td>
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<tr>
<td>30</td>
<td></td>
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<tr>
<td>40</td>
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<td>50</td>
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<td>60</td>
<td></td>
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<tr>
<td>70</td>
<td></td>
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<tr>
<td>80</td>
<td></td>
</tr>
</tbody>
</table>

Temperature range: 15°C - 35°C
4. Results (cont.)

4.2 Wafer banking (cont.)

<table>
<thead>
<tr>
<th>Screening item</th>
<th>Result of Screening</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Accept</td>
</tr>
<tr>
<td></td>
<td>Reject</td>
</tr>
<tr>
<td>Die shear test</td>
<td></td>
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<tr>
<td>Bond strength test</td>
<td></td>
</tr>
<tr>
<td>Internal visual and mechanical</td>
<td></td>
</tr>
<tr>
<td>DPA item</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Accept</td>
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<tr>
<td></td>
<td>Reject</td>
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<tr>
<td>Die shear test</td>
<td></td>
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<tr>
<td>Bond strength test</td>
<td></td>
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<tr>
<td>Life test item</td>
<td></td>
</tr>
</tbody>
</table>

Note (1) Lead with depression.

Result of Life test

<table>
<thead>
<tr>
<th>Life test item</th>
<th>Result of Life test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Accept</td>
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<tr>
<td></td>
<td>Reject</td>
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</tbody>
</table>

Result of DPA for the samples after completion of screening

<table>
<thead>
<tr>
<th>DPA item</th>
<th>Result of DPA for the samples after completion of screening</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Accept</td>
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<td>Reject</td>
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</tbody>
</table>

Result of DPA for the samples after completion of Life test

<table>
<thead>
<tr>
<th>DPA item</th>
<th>Result of DPA for the samples after completion of Life test</th>
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<tbody>
<tr>
<td></td>
<td>Accept</td>
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<td></td>
<td>Reject</td>
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</tbody>
</table>
5. Maintenance

5.1 LSI production system adopting COT

- Established LSI production system adopting COT for space application will be maintained.
- The typical samples will be manufactured and evaluated for the periodical QCI (Group C and D).
- More LSIs will be produced in the system:
  - Burst SRAM (same design rule as 320MIPS 64bit MPU)
  - SOI ASIC

- [Further details not provided]
5. Maintenance (cont.)

5.1 LSI production system adopting COT (cont.)

設計

設計データ

(HIREC & Customers)

検証

(HIREC)

出荷

(HIREC)

設計データ

(HIREC & Customers)

初期生産

ロット

(目標: 10年)

検査

ウエハ作製

(Multi-project-run methodology)

レイアウトA

レイアウトB

レイアウトC

ウエハ作製

(ワーフバンキング)

設置

製品ライン

設置

出荷

(専門会社)

評価データ

ウエハバンキング

(ワーフ保存 / チップ)

二つ以上のLSI

同じマスクに

5.1 LSI production system adopting COT (cont.)

- Cost can be reduced by applying LSI production system adopting COT.

Comparison of costs between Conventional LSI production system and LSI production system adopting COT:

- QC I
- Screening
- Assembly
- Wafer

![Diagram comparing costs between two LSI production systems.](image-url)
5. Maintenance (cont.)

5.2 Wafer banking

- Wafers will be evaluated periodically.
- At the beginning of storage.
- 2, 4, 7 and 10 years after storage.
- Other wafers (different design rule, substrate, etc.) will be evaluated for long-term storage.
### Maintenance (cont.)

#### Wafer Banking (cont.)

<table>
<thead>
<tr>
<th>Wafer (Design rule, Substrate)</th>
<th>Task</th>
<th>2003 FY (0H 0F)</th>
<th>2004 FY (0H 0F)</th>
<th>2005 FY (0H 0F)</th>
<th>2006 FY (0H 0F)</th>
<th>2007 FY (0H 0F)</th>
<th>2008 FY (0H 0F)</th>
<th>2009 FY (0H 0F)</th>
<th>2010 FY (0H 0F)</th>
<th>2011 FY (0H 0F)</th>
<th>2012 FY (0H 0F)</th>
<th>2013 FY (0H 0F)</th>
<th>2014 FY (0H 0F)</th>
<th>2015 FY (0H 0F)</th>
<th>2016 FY (0H 0F)</th>
<th>2017 FY (0H 0F)</th>
<th>2018 FY (0H 0F)</th>
<th>2019 FY (0H 0F)</th>
<th>2020 FY (0H 0F)</th>
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<td>Water A (0.18um, BULK)</td>
<td>Storage</td>
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<td>Water C (0.18um, Ep)</td>
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<td>Water D (0.18um, Ep)</td>
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<td>Water E (0.15um, SiGe)</td>
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*Storage, Assembly, Evaluation*
6. Information

EHIREC changed the company name on Oct. 25th, 2006.

High Reliability Engineering & Components Corporation
(Formerly: High-Reliability Components Corporation)

EHIREC homepage:
http://www.hirec.co.jp