European Space ASIC and FPGA, and efforts in Deep Submicron

European Space Agency (ESA)
Agustín Fernández-León
(ESTEC, TEC-ED, QC)
Summary

- European challenges of space ASIC and FPGAs
- Multi-project Wafer space programme
- ESA IP Cores service
- Standard ASICs and microprocessors
- European FPGAs
- Satcom drivers
- Efforts in Deep Submicron ASIC
- Contacts and additional info
European challenges of space ASIC and FPGAs

- Longer and more expensive ASIC developments (higher complexity of design & manufacturing)
- Rad-hardness, long term reliability
- Lack of flight heritage of new ASIC / FPGAs
- Costs/complexity of Space qualification of ASIC/FPGA
- Obsolescence or discontinuation of space qualified ICs
- Export constraints (e.g. US ITAR)
Multi-project wafer space programme

- **GOALS:** share mask/wafer costs, encourage first users (ESA funds the 4 first runs for 1.5M€)

- ATMEL (France) ATC18RHA CMOS 0.18µm, based on commercial process, hardened std-cell libraries, characterized and qualified with ESA and CNES support.

- ESA MPW contract with ATMEL (France):
  - 2004: set-up MPW technical and management procedures
  - 2005: successful “Validation Run” with 4 ASICs
  - 2007: 1st run with 2 ASICs (SpW-RTC, COLE)
  - 3 more runs pending (6 ASIC candidates identified)
## Multi-project wafer space programme

<table>
<thead>
<tr>
<th>MATRICES</th>
<th>Size (mm), Area (mm²)</th>
<th>Outer ring Programmable Pads</th>
<th>Inner ring typical number of array power pads</th>
<th>Buffer Power Supply Pads</th>
<th>Typical Nbr of Usable Gates</th>
<th>Typical Nbr of Usable Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATC18RHA95_220</td>
<td>6.19x6.19, 38</td>
<td>220</td>
<td>88</td>
<td>8</td>
<td>1 M</td>
<td>0.725 M</td>
</tr>
<tr>
<td>ATC18RHA95_324</td>
<td>8.76x8.76, 77</td>
<td>324</td>
<td>140</td>
<td>8</td>
<td>2.2 M</td>
<td>1.8 M</td>
</tr>
<tr>
<td>ATC18RHA95_404</td>
<td>10.66x10.66, 114</td>
<td>404</td>
<td>180</td>
<td>8</td>
<td>3.5 M</td>
<td>2.97 M</td>
</tr>
<tr>
<td>ATC18RHA95_504</td>
<td>13.03x13.03, 170</td>
<td>504</td>
<td>232</td>
<td>8</td>
<td>5.5-7.5 M</td>
<td>4.83 M</td>
</tr>
</tbody>
</table>
Multi-project wafer space programme

heavily pad limited ASICs:

- double pad rings in multi-deck cavity
Multi-project wafer space programme

✓ Package matrix combinations for Double Pad Ring (DPR):
  - MQFPF (160 to 352 leads)
  - MCGA (349 to 625 leads)

✓ buffers 70μm wide, pad pitch 95μm to:
  - Match the ceramic package bonding fingers pitch
  - Add decoupling capacitors for better noise filtering

✓ RHBD 3.3/2.5V IO buffers (cold sparing), SEE hard DFF
✓ 400MHz+ PLL
✓ LVDS ref pads with internal cluster-routing to save pads and pins
✓ Available space quality grades: ESCC & QML Q/V
✓ Available with the SMD 5962-06B02
✓ European Preferred Parts List (EPPL) 1 listed
✓ E QML certification by 2H08
Multi-project wafer space programme

Validation run (2005)

1st run (2007)

Lessons learned:
- fewer ASIC designs ready per year (1 run per year, and not 2 as initially expected)
- difficult to have two or more ASICs ready for tape-out at the same time
- MPW run dates/deadlines are difficult to set to satisfy everybody’s project needs
- to avoid waiting, some opt for mono-project or their own MPW despite higher costs
ESA IP Cores service

**GOALS:**

- cheaper, faster multi-IP/S-o-C designs (by VHDL re-use)
- availability of key digital functions for space in “soft format” = “technology portable”
- mitigate effects of Standard ASIC components/technology discontinuation by foundries (e.g. porting to another technology)
- promote/facilitate use of standardised (e.g. ECSS) functions/communication protocols/system architectures
- centralise IP users’ feedback to improve quality of existing IPs and identify future needs
ESA IP Cores service

ESA IP Cores available

- SpW-b, SpW-AMBA [SpaceWire CODEC]
- LEON2-FT (Fault Tolerant 32bit SPARC)
- CAN [Controller Area Network]
- PTME [CCSDS Packet Telemetry Encoder]
- PDEC, PTCD [CCSDS Packet Telecommand Decoder]
- EDAC [Error Detection And Correction Encoder/Decoder]
- OBDH [On-Board Data Handling]
- CUC-CTM [CCSDS Unsegmented Code & Time Manager]
- EVI32 [32-bit VMEbus interface for the ERC32 processor chip set]
- WIC [Wavelet Image Compression]
- IP1553 [Mil-Std-1553 interface]

Each IP core delivery
- Documentation, VHDL source code, Test-benches, Simulation and synthesis scripts
ESA IP Cores service

- Specific licence conditions for each IP Core
- Only distributable within ESA member states (some have a parallel commercial distribution)
- Free for use in ESA projects
- ESA IP Cores website:
  http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html
ESA IP Cores service

Number of IP Core requests statistics (September 2008)
Standard ASICs

Space qualified ASICs that are sold as standard products, with third party technical support (by designers-foundry contract)

**GOALS:**

- cheaper, faster space system designs (by ASIC re-use)
- availability of key functions for space in “hard format” = “already manufactured, tested and qualified”
- promote/facilitate use of standardised (e.g. ECSS) functions, communication protocols and system architectures
- collect ASIC users’ feedback to identify present (corrected Data Sheets), and future needs (redesigns, second generations)
Standard ASICs and products

All with ATMEL 0.5, 0.35 or 0.18µm

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT697E (*)</td>
<td>LEON2FT 32bit SPARC engineering and QML-Q flight models</td>
</tr>
<tr>
<td>AT7909E</td>
<td>(SCTMTC) Single Chip TeleMetry and TeleCommand</td>
</tr>
<tr>
<td>AT7910E</td>
<td>(SpW-10X) SpaceWire Router.</td>
</tr>
<tr>
<td>AT7911E</td>
<td>(SMCS332SpW) Scalable Multi-channel Communication Subsystem I/F between 3 SpaceWire links, central data processing unit and communication data memory.</td>
</tr>
<tr>
<td>AT7912E</td>
<td>(SMCS116SpW) I/F between 1 SpaceWire link and data i/f: ADC/DAC, RAM, FIFO, GPIO's, UARTs.</td>
</tr>
<tr>
<td>T7906E</td>
<td>(SMCS lite) Single Point to Point IEEE 1355 High Speed Controller</td>
</tr>
<tr>
<td>TSS901E</td>
<td>(SMCS332) Tripple Point to Point IEEE1355 High Speed Controller</td>
</tr>
<tr>
<td>TSC695 (*)</td>
<td>(ERC32 single chip) Rad hard SPARC single chip processor</td>
</tr>
<tr>
<td>TSC21020F (*)</td>
<td>Rad Hard 32-bit floating point DSP</td>
</tr>
<tr>
<td>T79055 (**)</td>
<td>(AGGA2) Advanced GPS/GLONASS ASIC</td>
</tr>
</tbody>
</table>

(*) Standard Microprocessors products  (***) Not in catalogue, but available with ESA authorisation
Standard ASICs and products

Under development (ATMEL 0.18µm and STMicroelectronics 65nm):

- AT697F (*) LEON2FT Flight Model (protos Q3-2008)
- AT7913E (SpW-RTC) SpaceWire-Remote Terminal Controller (protos Q4-2008)
- XXXXXXX (**) (SCOC3) Spacecraft Controller on a Chip (protos Q2-2009)
- XXXXXXX (**) (FFTC) Fast Fourier Transform Coprocessor (protos Q2-2009)
- XXXXXXX (**) (HSSL) High Speed Serial Link ASIC (protos 2010)
- XXXXXXX (**) (CICA) CCSDS Image Compression ASIC (2011)
- XXXXXXX (**) (NGMP) Next Generation Multi-purpose Processor (2011)
- XXXXXXX (**) (AGGA4) Advanced GPS/GALILEO ASIC
- XXXXXXX (**) Next Generation DSP

(*) Standard Microprocessors products  (**) Candidate for standard ASIC not approved yet
European FPGAs

ACTEL, XILINX, ATMEL FPGAs capacity evolution
(Memories and Hard Macros excluded)

- RTSX (0.25 μm)
- AT40KE (0.35 μm)
- QPRO-R Virtex (0.15 μm)
- QPRO-R Virtex-II (0.22 μm)
- RTAX (0.15 μm)
- QPRO-R Virtex-4 LX (90 nm)
- SIRF Virtex-5 (65 nm)
- AT280F (0.18 μm)
- RT3PE (*) (0.13 μm?)

Note: (*) Flash-based. Predicted value TBC
European FPGAs

ACTEL vs ATMEL FPGAs capacity evolution

(Memories and Hard Macros excluded)

(*) Flash-based. Predicted value TBC
European FPGAs

ATMEL FPGAs evolution

- AT40KEL (0.35 μm)
- AT280F (0.18 μm)
- AT700 (0.15 μm)
- AT1000 (90 nm?)
- AT2000 (90 or 65nm?)

Roadmap Dependencies
New EDA/CAD tools

Capacity (Kgates)


CMOS SEU Hardened OKI SOI
European FPGAs

CNES and ESA are supporting European reprogrammable space FPGA developments, based on ATMEL expertise and technology, with JAXA/HIREC/OKI support

- 40K & 280K gates FPGA DK capabilities evaluation (for ESA IP Cores) (ESA Funding)
- FPGA/SOI Validation Phase (ATMEL/OKI/HIREC) (CNES Funding)
- 280 Kgates FPGA + 4 Mbit EEPROM in one package (CNES Funding)
- Reprogrammable Computer in one package: LEON2 AT697F + 280 Kgates FPGA in one package (CNES Funding)
- FPGA 280Kgates ESCC Evaluation (ESA Funding)
- FPGA/SOI 360 Kgates development (JAXA/CNES/ATMEL/OKI/HIREC) (CNES + JAXA Funding)

- **Challenge:** to raise funding for >1Mgates European space reprog. FPGA. Negotiations at different levels on-going
Telecom satellite drivers

Drastic reduction of mass/volume and power consumption, higher sampling speeds needed

Short/Medium Term:

Narrowband L/S-band Digital Processors: mobile processors (e.g. Inmarsat4, Alphasat), 200 MHz processed bandwidth, digital sub-channelizer

Medium/Long Term:

Ku/Ka-band Broadband Digital Processors: new products with a processed bandwidth > 25 GHz (at least 100 times Inmarsat4 !) + Active antennas with digital beam forming
Telecom satellite drivers

**High Data Rate Transfer Between Functions**

- **A/D 1.25GSp 10 bits**
  - 12.5 Gbps
  - 625 MHz

- **Demux 50-way o/s ×2**
  - 18 Gbps
  - 40 MHz

- **Mux 50-way**
  - 12.5 Gbps
  - 100 MHz

- **D/A 1.25GSp 10 bits**
  - 1 Gbps
  - 100 MHz

**Spatial Switch**

- 4000 × 4000
- 12.5 MHz granularity
- o/s ×2
- 9+9 bits

**Core Signal Processing**

- **Hundreds of ASICs**

**1 Unit: FWD or RTN Processor**

**200 Converters**

**1.8 Tbps Throughput**
Telecom satellite drivers

Technology Impact on Narrowband/Mobile Processors Power Consumption

- Current European space qualified technology
- Inmarsat IV = 1kW/Unit (0.65 µm Honeywell technology)
- US Flying techno SpaceWay (IBM Asics 0.16 µ m)

Power Consumption per Unit [W]

Technology Evolution

- Unit = FWD or RTN Processor
- 0.18 µm Parallel links Current ADC/DAC
- 0.18 µm Parallel links New ADC/DAC
- 0.13 µm Serial links New ADC/DAC
- 90 nm Serial links New ADC/DAC
- 65 nm Serial links New ADC/DAC
- 110 nm Serial links New ADC/DAC

- More than a factor 2 improvement wrt. I4
- Improvement from 90 nm to 65 nm is more marginal in terms of power consumption
- US Advertised Technology (LSI 110 nm, IBM 65 nm)
### Telecom satellite drivers

Requirements identified with the main SatCom European primes (EADS, Thales Alenia Space), Agencies (ESA, CNES) and main technology vendors and foundries for:

<table>
<thead>
<tr>
<th>Component</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC Technology</td>
<td>✓ 90 nm or 65 nm ✓ &gt;600 pins, Flip-Chip ✓ ~20Mgates, 10W/cm² disipation</td>
</tr>
<tr>
<td>ADC</td>
<td>✓ &gt; 1.5 Gsps ✓ 10 bits ✓ Power ~ 1.1W</td>
</tr>
<tr>
<td>DAC</td>
<td>✓ &gt; 1.5 Gsps ✓ 12 bits ✓ Power ~ 0.5W</td>
</tr>
<tr>
<td>High-Speed Serial Links</td>
<td>✓ 6.25 Gbps ✓ Power ~ 150 mW/Gbps per transceiver</td>
</tr>
</tbody>
</table>

Better fit with manufacturers roadmap

Encompass mobile and broadband applications
New contracts!

**Efforts in Deep Sub Micron**

- **Phase 1**
  - First iteration
  - Design / prototyping
  - T.R.L 3/4
  - TRP Budget 1.2M€

- **Phase 2**
  - Second iteration
  - Design / prototyping and ESCC evaluation
  - T.R.L 5
  - T.R.L 8

- **Phase 3**
  - Qualification according to ESCC standards
  - T.R.L 8

**ASIC Technology**
- Harden library
- High speed serial link
- High pin count package

**Analog to Digital Converter**
- T.R.L 4
- TRP Budget 0.9M€

**Digital to Analog Converter**
- T.R.L 4
- TRP Budget 0.9M€
Efforts in Deep Sub Micron

Deep Sub-Micron ASIC and HSSL development

ESA (TRP) contract

Activity duration 24 Months
Cost 1.2 M€
Kick off February 2008

STMicroelectronics (France)
ISD (Greece) + Thales Alenia Space (F) + EADS Astrium (UK)

Phase 1A Feasibility study (end Nov 2008)
- Specs for future ASIC platform
- Specs for High Speed Serial Links (HSSL)
- Reliability and radiation assessment of ST 65nm
- Design solutions for reliability enhancement and radiation mitigation
- Compliance between ST qualification flow and ESCC procedures
- Identification of high pin count package solutions for future ASIC platform

Phase 1b HSSL Design / prototyping (end Mar 2010)
- Definition of library cells needed for future ASIC platform and HSSL
- 6.25 Gbps HSSL architecture study
- HSSL design: Quad HSSL on same die (25 Gbps)
- HSSL prototyping
- HSSL characterisation: electrical / radiation / reliability
- Commercial study and market prospective
Efforts in Deep Sub Micron

Deep Sub-Micron ASIC and HSSL development

ESA (TRP) contract

- “Structured ASIC” solution based upon STMicroelectronics 65 nm GP CMOS low power

  - Dual/triple gate oxide
  - Copper interconnect
  - 7 metal layers
  - 5.7 nW/MHz/gate

  - 0.20 µm metallization pitch
  - 750 kgates / mm2 for standard cell libraries
  - 2 GHz standard cells
  - High speed serial link IP performing up 7.5 Gbps

Main functions (logic, memory, I/O buffers, HSSL …) pre-engineered on base layer
device customised with top few metal layers
Less engineering efforts for “lower” cost ASIC
Efforts in Deep Sub Micron

65 nm under radiation effects
• Rad-hard capabilities measured under ESA-ST contracts (ST 130nm, 90nm, 65 nm), no show stopper identified so far
• Usage of an optional mask layer for SEL mitigation
• Re-use of SEU mitigation techniques (ST patented)
• Cells and clock-trees specifically developed for 65 nm platform
• rSRAM (robust SRAM) developed and patented
• Rad-hard by design know how enriched by end users cooperation (CERN, CEA-LETI, EADS).
Efforts in Deep Sub Micron

Other DSM contracts:

• Design Against Radiation Effects (DARE) on UMC 180nm & 90nm
test vehicle and lib development for UMC 90nm, maintenance and ESCC
qualification (based on LEON3FT ASIC) of existing DARE180nm
[IMEC(B), ETCA(B), Gaisler Research(Sweden)]

• Radiation Effects in DSM CMOS
Simulation Framework toolkit for IC designers to characterize impact of radiation
effects on DSM ICs. Characterization by theoretical analysis and 3D simulation of
SEE and TID, and new effects and trends in DSM. <100 nm CMOS.
Contacts / Additional info

ESA Microelectronics Section
http://www.esa.int/TEC/Microelectronics/index.html

ESA IP Cores
http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html

Atmel hotline and web announcement for SMPW, and Rad Hard ICs
smpw-atc18@nto.atmel.com
http://www.atmel.com/dyn/resources/prod_documents/ATC18RHA_SMPW.PDF

SpaceWire
http://spacewire.esa.int

ECSS-Q60-02: ASIC and FPGA development
http://www.ecss.nl/
https://escies.org/ReadArticle?docId=167

European Space Components Information Exchange System
https://escies.org/
THANKS

for your attention and questions

Thanks to ESTEC TEC-ED, QC colleagues, CNES, ATMEL, ST and ESA contractors for all their inputs for this presentation

European Space Agency (ESA)
Agustin.Fernandez-Leon@esa.int
Complementary slides on some Standard ASICs, Standard microprocessors and FPGAs
Standard products

**ERC32 processor**

**TSC695F(L)**

- Sparc V7 RISC architecture
- Rad hard 300 KRADs (Si), < 3 E-8 Error/Comp/Day, No SEL LET 80 MeV/mg/cm2
- 20 Mips / 5 MFlops at 25 MHz ; 230 mA ; 5V ± 0.5V
- Large High Flight heritage (Launchers – telecomm & scientific satellites, Europe: SMART-1 lunar mission, Alcatel Spacebus satellite platforms, Galileo...; USA: Deep Impact, Mars Reconnaissance Orbiter...)
- 3.3V version available (TSC695FL)
- 12 Mips ; 100 mA
- Package: 256 MQFPF; Bare Die
Standard products

LEON2FT processor Engineering Model

AT697E

- RISC / Sparc V8 LEON2-FT Integer and FPU
- Embedded Icache: 32Kbytes; dcache: 16 Kbytes
- SDRAM memory controller
- PCI 2.2 interface (33 MHz)
- At 100MHz: 86 MIPS (Dhrystone 2.1), 23 MFLOPs
- Power consumption 7 mW / MHz
- At 100 MHz / worst case: core 0.5 W, I/O 0.2 W
- CMOS ATC18 0.18 micron; 1.8 V core; 3.3V I/Os
- Fault tolerance by design (TMR with skew for SEU and SET protection)
- EDAC on register files and external memories & Parity on the caches
- No SEL LET 95 MeV/mg/cm² – max voltage – 125°C; TID 200 krad (Si)
- Multi Column Grid Array (MCGA) 349, and MQFP 256
Standard products

LEON2FT processor (Flight Model) AT697F

- VHDL model bug corrections + a few functional improvements
  - New write memory block protection, easier to use
  - Simplified 8-bit memory EDAC scheme (boot)
  - Counters extended to 32 bits
  - Four additional interrupts
  - Asynchronous sampling of BRDYN signal + extension to PROM, to ease the interfacing with external devices
  - Higher SDRAM interface speed
- ATC18RHA library (RHA process reliability monitoring) and better TID 300 krad (Si) + full space qualification
- Pin out compatible with AT697E
- Multilayer Quad Flat Pack (MQFP) 256 pins package, in addition to (MCGA) 349 package
- Protos under testing now! FM parts expected for 2009
Standard ASICs

SCTMTC AT7909E

- Re-definable by the use of different mission PROM
- Supports multiple sources of CPDU segments
- Packet wire or Space Wire control interface
- Can use either 8- or 16-bit PROM and RAM
- 3.3V supply voltage
- Operating frequency : 16 MHz
- Maximum frequency : 22.2 MHz
- Technology MH1RT 0.35μm
  - Radiation Hardened CMOS process
  - No SEL below LET threshold of 70 MeV/mg/cm
  - SEU hardened flip-flops
  - Functional and parametric TID 200 krads (Si).
- Package : 256-pin QFP package.
- Quality flows : Military and Space level

MEWS 21
Standard ASICs

SpaceWire -10X Router

AT7910E

Device

- Non-blocking routing switch for SpW packets, time code distribution
- RMAP support
- 8 SpW, 1 parallel, 1 config. ports
- Radiation tolerant gate array technology from Atmel: MH1RT (0.35 µm)
- 196 pins, MQFP
- Power consumption @ 3.3V:
  - 1.5 W @ 10 Mbit/s TBC
  - 5.1 W @ 200 Mbit/s TBC

Industrial Partners

- EADS Astrium (D)
- Austrian Aerospace (A)
- University of Dundee (UK)
- Atmel (F)
Standard ASICs

SMCS332SpW
AT7911E

Device
- 3 SpW interfaces for intelligent nodes
- Radiation tolerant gate array technology from Atmel: MG2RT (0.5 µm)
- 196 pins
- Power consumption: 1.7 W
- 3.3V version: 100Mbit/s
- 5 V version: 200Mbit/s

Industrial Partners
- EADS Astrium (D)
- Atmel (F)
Standard ASICS

SMCS116SpW
AT7912E

Device
- 1 SpW interfaces for simple nodes
- Radiation tolerant gate array technology from Atmel: MG2RT (0.5 µm)
- 100 pins
- Power consumption SMCS116 SpW max:
  - 216 mW @ 3.6V
  - 660 mW @ 5.5V
- Power consumption external LVDS transceiver:
  - 70 mW @ 3.3V per SpW interface
- 3.3V version: 100Mbit/s
- 5 V version: 200Mbit/s

Industrial Partners
- EADS Astrium (D)
- Atmel (F)
Standard ASICs

**SpW-RTC**

**AT7913E**

- **Device**
  - Leon2 FT+FPU, CAN-Bus, 2*SpW,
  - FIFO, ADC, DAC, UART
  - SW can be uploaded via SpW link,
  - RMAP compatible
  - ATC18RHA (0.18 µm)
  - MCGA 349
  - 1.8V core, 3.3V I/O
  - SpW link speed up to 200Mbit/s
  - FM expected for Q2 - 2009

- **Industrial Partners**
  - Saab Space (S)
  - Gaisler Research (S)
  - Atmel (F)
Standard ASICs

LEON3-FT SPARC V8 processor macro including DSU, MMU and GRFPU-FT

2x1553 BC/BM/RT modules, two CAN modules
TC decoder module, TM encoder module
Housekeeping module, CCSDS Time Management,
7 Spacewire modules,
4 UARTs modules (3 APB UART and 1 AHB UART),
Two memory controllers (SDRAM, SRAM, EEPROM),
AHB bus monitoring module, Two AHB status module
DMA Telemetry,
Bridge & DMA between 2 AHB busses
A Switch Matrix module
IRQ controller, timers, GPIOs
FPCTL module
ATC18RHA 0.18µm / MCGA 472 Ceramic
First protos Q2-2009
Standard products

Next Generation Multipurpose Processor

- 400 MIPS minimum
- Standard product implemented in DSM CMOS (STMicroelectronics 65 nm is today’s baseline)
- SPARC compliant multi-core architecture
- MMU, debug support unit, large on-chip memory (16-32 kB)
- Standardized interfaces like 1553, SpW, CAN and RS422
- Interface to co-processors and companion chips

Invitation to Tender goes out Q4-2008

Next Generation Space DSP

- 1 GFLOPS minimum performance
- Radiation hardened design, small footprint, low power
- Easy interfacing to standard DSP system components (ADC/DAC, memories, onboard networks, DSP arrays)
- High quality software development environment
- Availability as a space qualified standard component

TSUKUBA Oct 6th, 2008  slide: 41
European FPGAs

AT40KEL040

Atmel development funded by CNES

46K gates equivalent ASIC gates
20 MHz clock speed
2304 core-cells (each 2 LUT + 1 DFF)
18 Kbit SRAM (FreeRAM) 144 modules of 32x4
3.3V Core and I/Os with 5V-tolerance
MQFPF-160 (129 User I/O)
MQFPF-256 (233 User I/O)
AT56KRT 0.35µm technology
All memory points are SEU hardened:
- Core-cell DFF / FreeRAM
- Configuration Memory & Controller
TID tested up to 300 Krad
7 E-5 error/device/day in GEO
European FPGAs

**ATF280E**

Atmel development funded by CNES

- 280K equivalent ASIC gates
- 50 MHz clock speed
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit SRAM/TPRAM (900 modules of 32x4 blocks)
- LVDS: 8 Rx + 8 Tx
- MCGA 472 (308 User I/O) / MQFP-256 (150 User I/O)
- Configuration load & self-integrity check
- CMOS 0.18µm, Cold-sparing and 3.3V PCI-compliant I/Os
  - SEU Fault-Tolerance by design
  - SET hardening (clocks and reset)
  - TID up to 300 Krad
- 1 E-6 error/device/day in GEO

**AT69170E**: rad-hard serial EEPROM (4 Mbit) serial FPGA configuration download

- 5 E-7 error/device/day GEO, TID expected 60 Krad, Endurance: 10K cycles, Data retention: 10 years
- Atmel development supported by ESA