Development Status for JAXA Critical Parts, 2008

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Background

- Increased demands for high performance space systems
- Increased cost for LSI fab.
- Decreased availability of cutting edge devices for space applications.

Mismatch of demand and supply

Critical parts for space systems were selected to develop advanced space systems by Space Parts Engineering Committee.

Overall status (1st phase Critical parts 1/2)

Parts for high performance computer system.

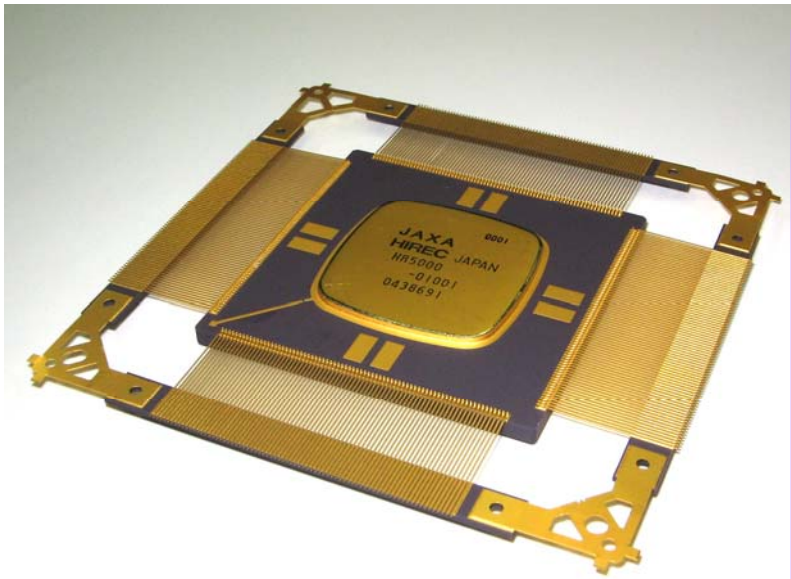
- High performance Microprocessor (64bit MPU)
  - ➡ QT was successfully completed in 2007.
  - ➡ Feasibility is started to realize the performance improvement by SOI.
- Synchronous memory (Burst SRAM)
  - ➡ QT was successfully completed in 2008.
- SOI ASIC / FPGA
  - ➡ It is scheduled to start the entire FPGA design in the last half of FY2008.
  - ➡ ASIC library will be released in FY2008.

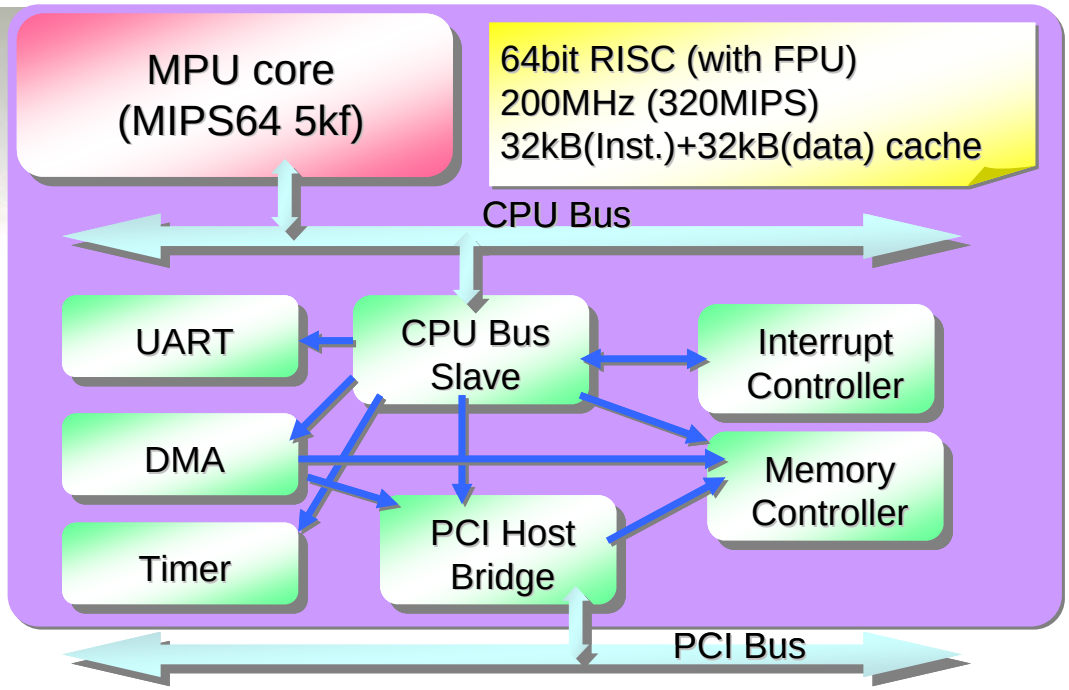
Overall status (1st phase Critical parts 2/2)

Parts for high reliability power supply system.

- DC/DC converter
  - ➡ QT was successfully completed in 2007.
- POL (Point of load)
  - ➡ Element evaluation (Control ICs, Trench type Power MOSFET) is in progress.
  - ➡ QT will be completed in next fiscal year.
- Power MOSFET
  - ➡ QT was completed (n-ch, 100-500V).
  - ➡ Development of p-ch type is in progress. (QT will be completed in FY2010)

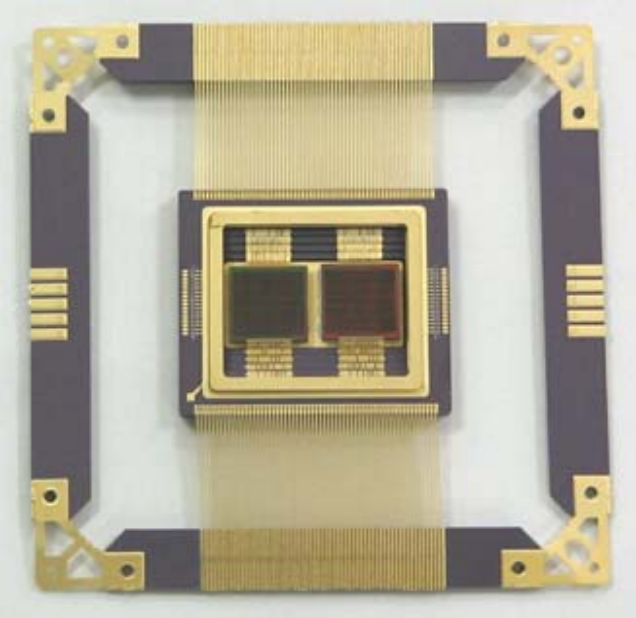
320MIPS 64bit MPU for space

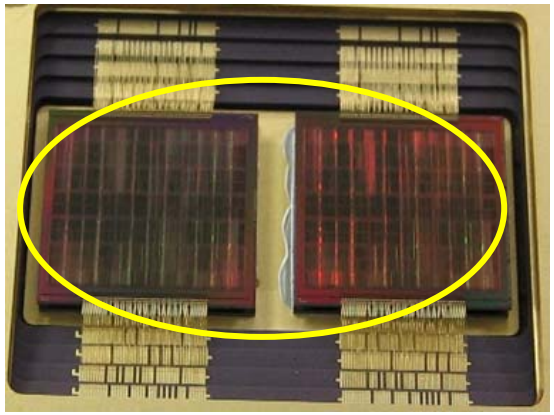




- MIPS64 5kf architecture with on-chip peripherals.
- 0.18μm commercial CMOS process.
- 200MHz operation (320MIPS)
- JAXA qualified. (Mar. 2007)

36M bit burst SRAM for space

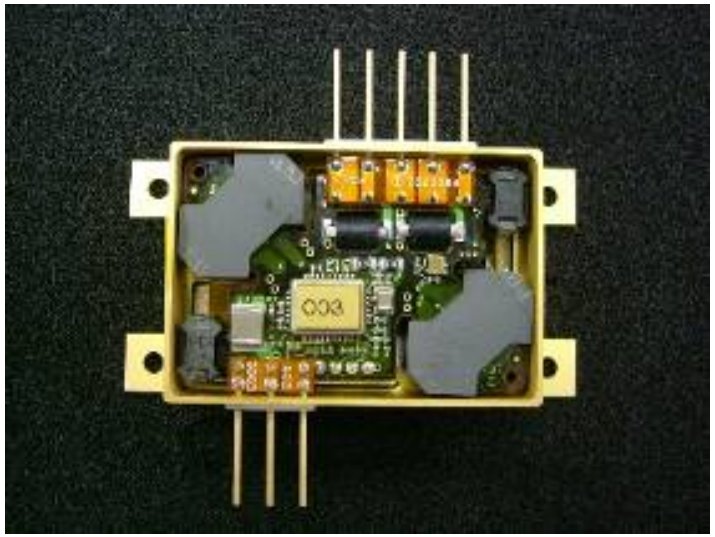




Multi chip
(18bit x 512k x 4chip)

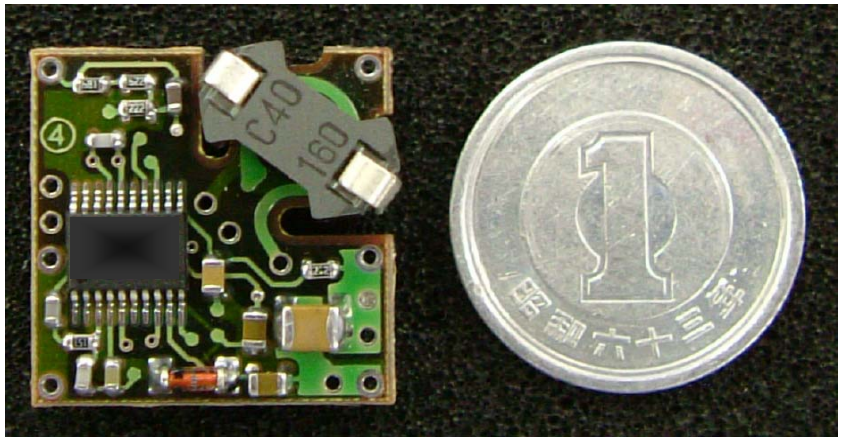
- 36Mb, 72(64 data and 8 ECC)-bit x 512k-word
- 100MHz synchronous operation.
- Separated address decoders and cell blocks to prevent multi-bit SEUs in a word.
- JAXA qualified (Mar. 2008)

DC/DC converter and POL



- Unique structure with no magnet wires for chokes/transformers.
- Direct connection to 28V/50V unregulated bus. (+/- 15V output)

- Direct connection to +15V output of DC/DC converter to produce 1.5V, 1.8V, etc.
- Small, High efficiency

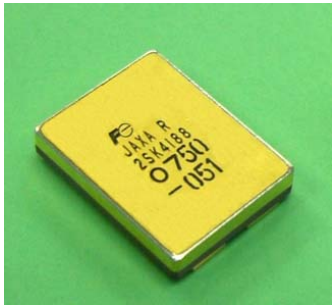


Power MOSFET (n - channel)

- SEB/SEGR Hardened up to 100% $V_{(BR)DSS}$
- Lowest $R_{DS(ON)}$, Patented structure

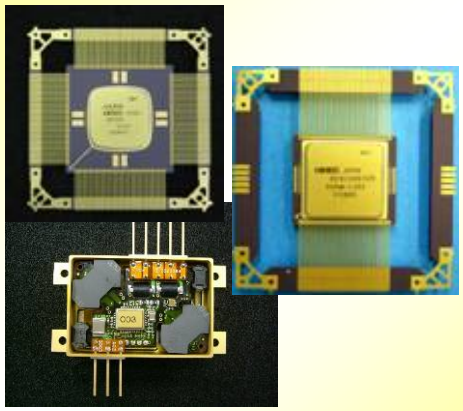
	TO-254			SMD			
	Parts	I_D (A)	R_{on}	Parts	I_D (A)	R_{on}	Package
100V	2SK4048	42	18mΩ	2SK4217	42	13mΩ	SMD-2
	2SK4049	42	33mΩ	2SK4218	39	28mΩ	SMD-1
	2SK4050	15	69mΩ	2SK4219	15	64mΩ	SMD-0.5
130V	2SK4214	42	24mΩ	2SK4152	42	17mΩ	SMD-2
	2SK4215	35	46mΩ	2SK4153	42	39mΩ	SMD-1
	2SK4216	15	96mΩ	2SK4154	15	89mΩ	SMD-0.5
200V	2SK4051	42	33mΩ	2SK4155	42	26mΩ	SMD-2
	2SK4052	33	69mΩ	2SK4156	32	62mΩ	SMD-1
	2SK4053	14	155mΩ	2SK4157	14	148mΩ	SMD-0.5
250V	2SK4054	42	45mΩ	2SK4158	42	38mΩ	SMD-2
	2SK4055	27	98mΩ	2SK4159	26	91mΩ	SMD-1
	2SK4056	12	230mΩ	2SK4160	12	223mΩ	SMD-0.5
500V	2SK4185	23	180mΩ	2SK4188	23	180mΩ	SMD-2
	2SK4186	10	480mΩ	2SK4189	10	480mΩ	SMD-1
	2SK4187	4.5	1150mΩ	2SK4190	4.5	1150mΩ	SMD-0.5

TO-254

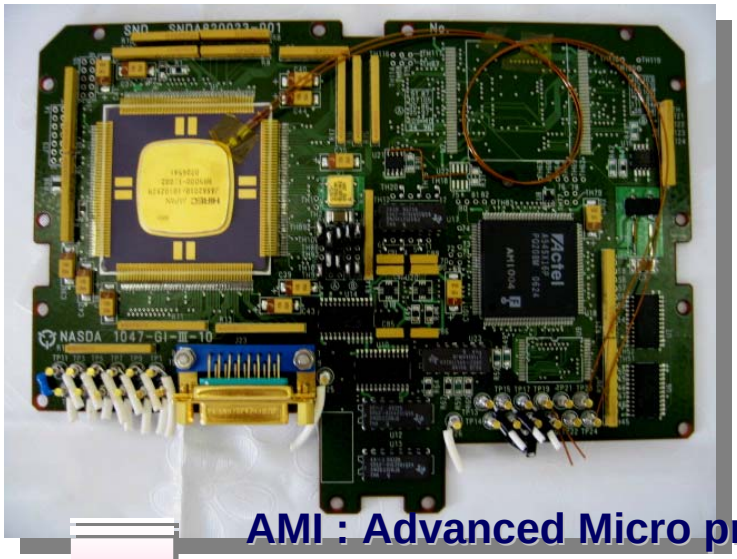


SMD

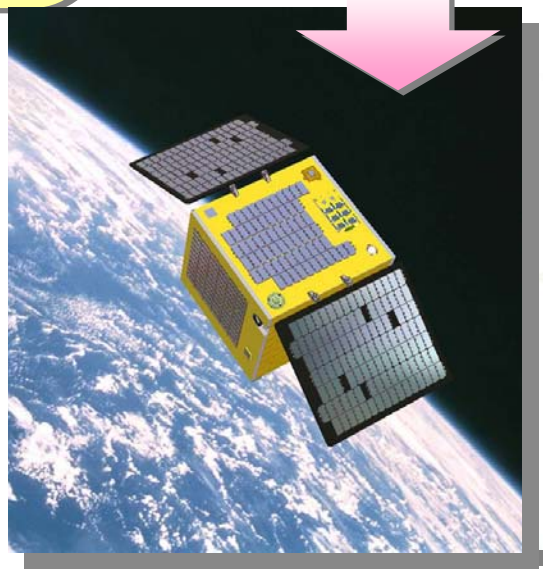
Flight demonstration (SDS-1)

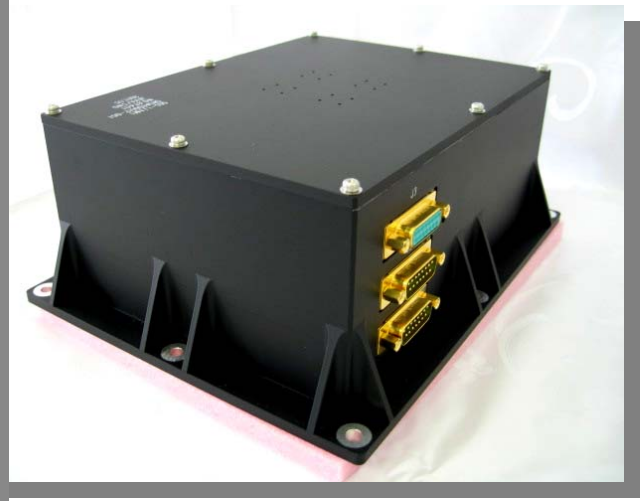


1st phase critical parts



AMI : Advanced Micro processing In-orbit experiment equipment

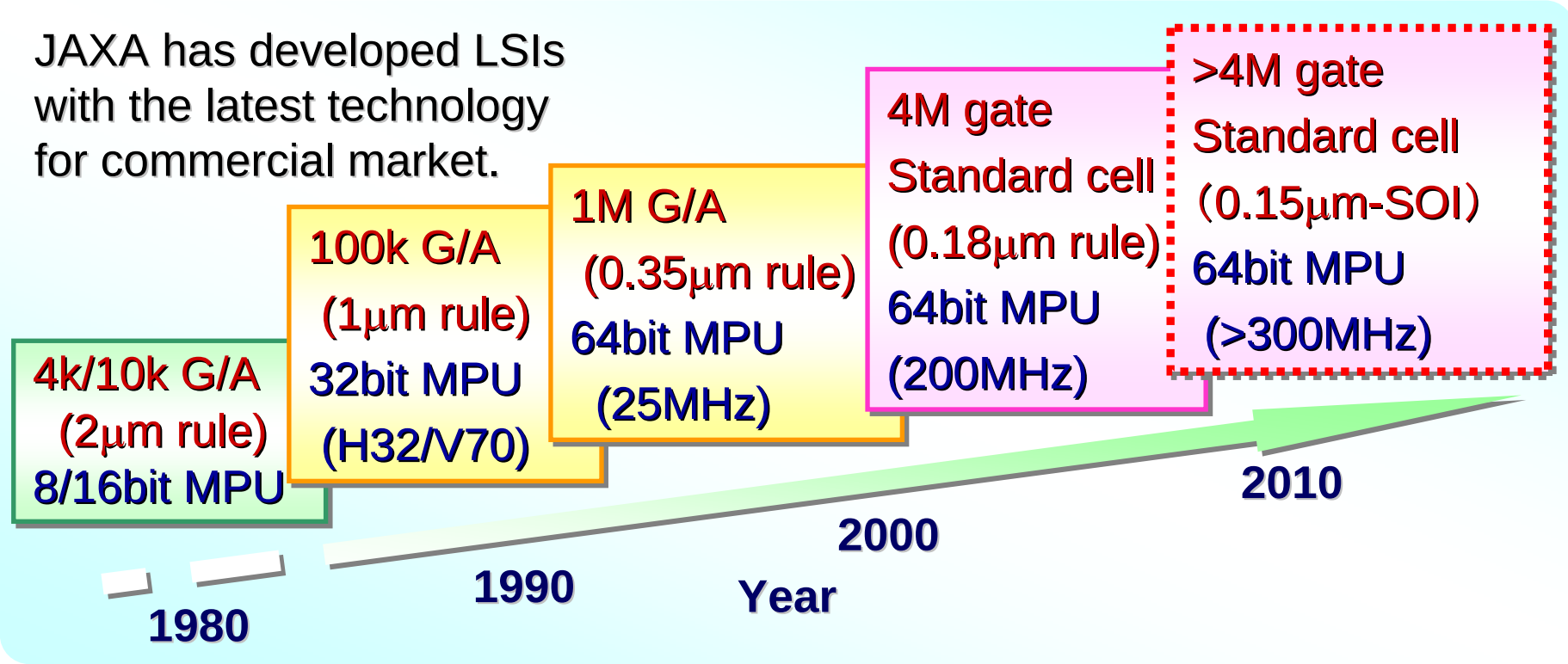




SDS-1 : Small Demonstration Satellite #1

SDS-1 is scheduled to be launched in FY2008.

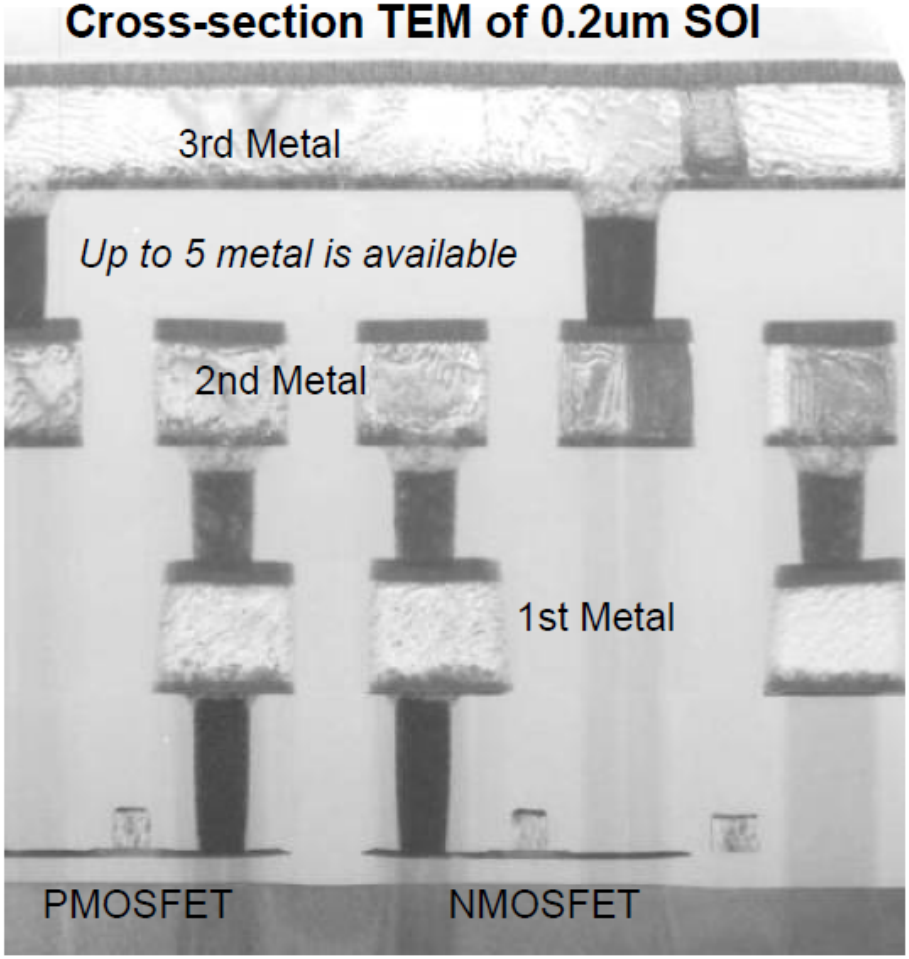
JAXA's LSI (MPU/ASIC) roadmap



For <0.18μm technology, SEEs are main concern for LSIs for space applications. FD-SOI is attractive for space because of its SEE hardness as compared with bulk technology.

Oki FD-SOI Device Structure & Process

Cross-section TEM of 0.2um SOI



- Lpoly = 0.2 mm
- SOI Thickness under Gate = 50nm

Substrate : BONDED WAFER

◆0.35um SOI Process
- Gate length : 0.35um
- Gate Oxide thickness : 7nm
- Wiring Pitch : 1.4um

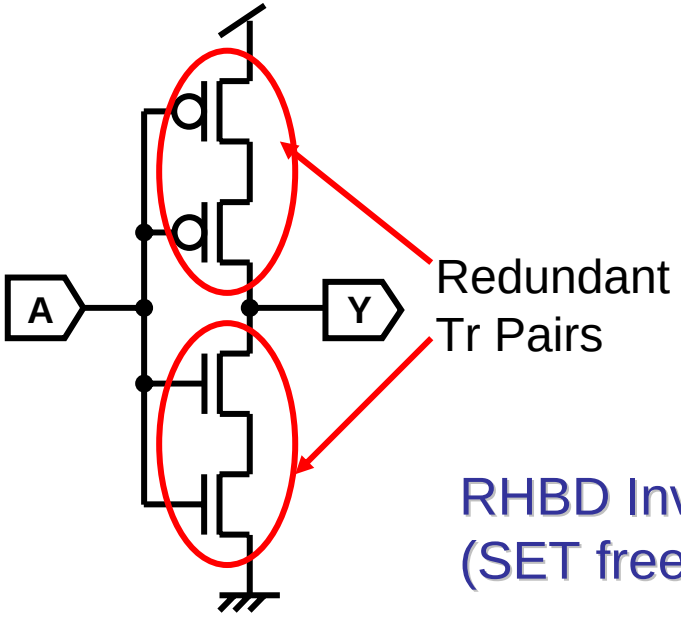
◆0.2um SOI Process
- Gate length : 0.2um
- Gate Oxide Thickness : 4.5nm
  4.5nm/7nm for 3.3V
- Wiring Pitch : 1.0um
- MIM, Inductor

◆0.15um SOI Process (shuttle)
- Gate length : 0.14um
- Gate Oxide Thickness : 2.5nm
- Wiring Pitch : 0.52um
- MIM, Inductor

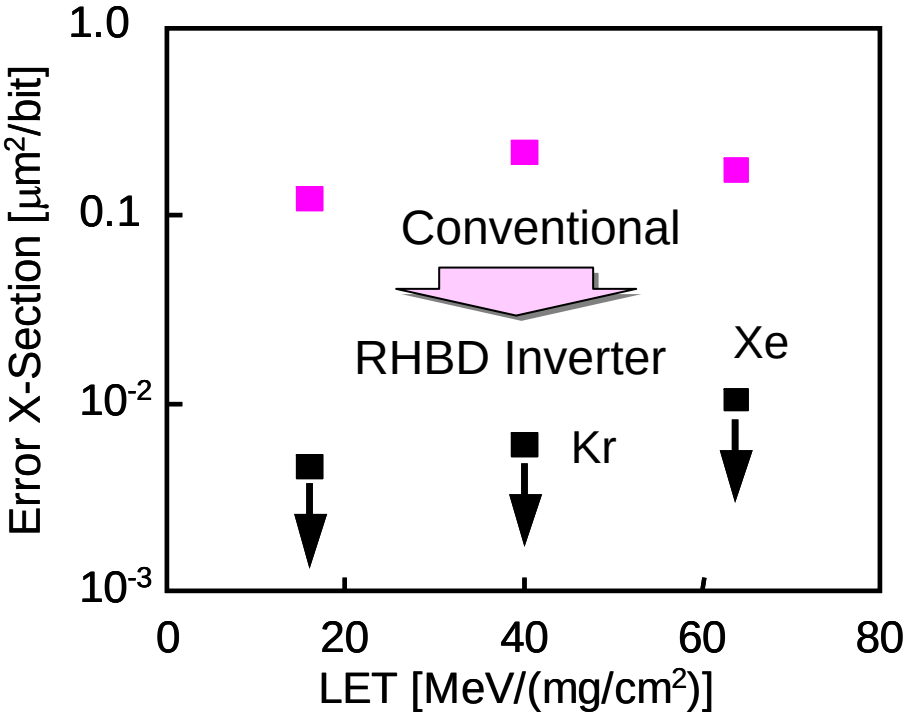
⇨ **- 0.15um SOI (Production line)**
LOCOS ⇒ STI
Metal 0.52 ⇒ 0.39(1M)/0.48(<2M)
BOX 200nm ⇒ 145nm
Low Leakage (LL) Ioff<2E-12A/um

(Courtesy of OKI, quoted from 19MEWS material)

Basic concept of RHBD

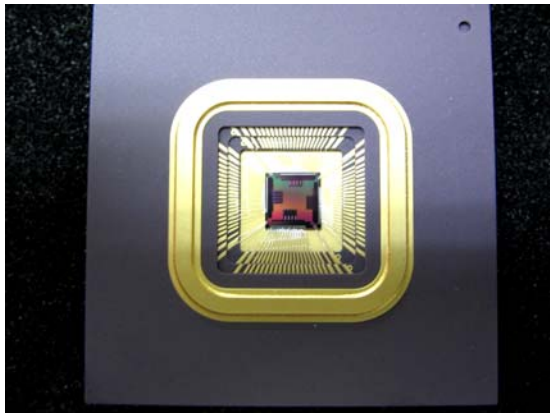


RHBD Inverter
(SET free)



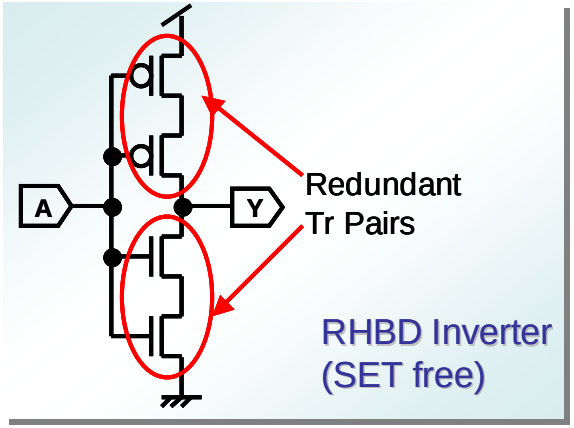
The redundant transistor pairs completely prevent the SET pulse generations on the output terminal.This concept can be easily extended for any logic gates and the logic circuits. However the optimization of area, power, speed penalties is an important issue.

Application of SOI technology for space

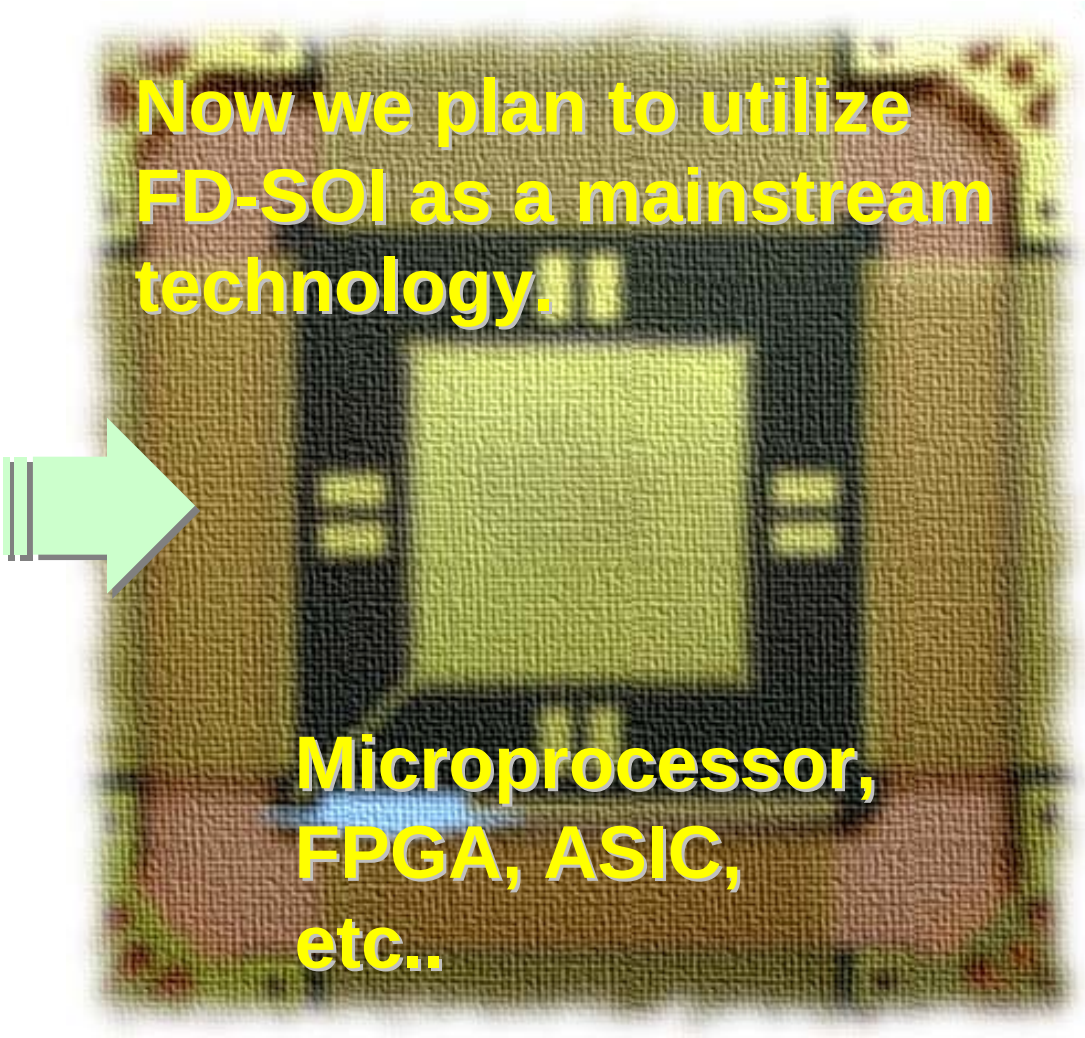


0.15μm FD-SOI

+



RHBD techniques
(RHBD Cell library)



Target Specification for ASIC / FPGA

- 0.15 μ m commercial FD-SOI foundry with patented SEU/SET free primitive circuits. (RHBD techniques used)
- 1.5V for core and 3.3V for I/Os.
- SEU/SET free up to LET of 64MeV/(mg/cm^2)
- TID: 1kGy(Si) (100krad(Si))

ASIC & FPGA

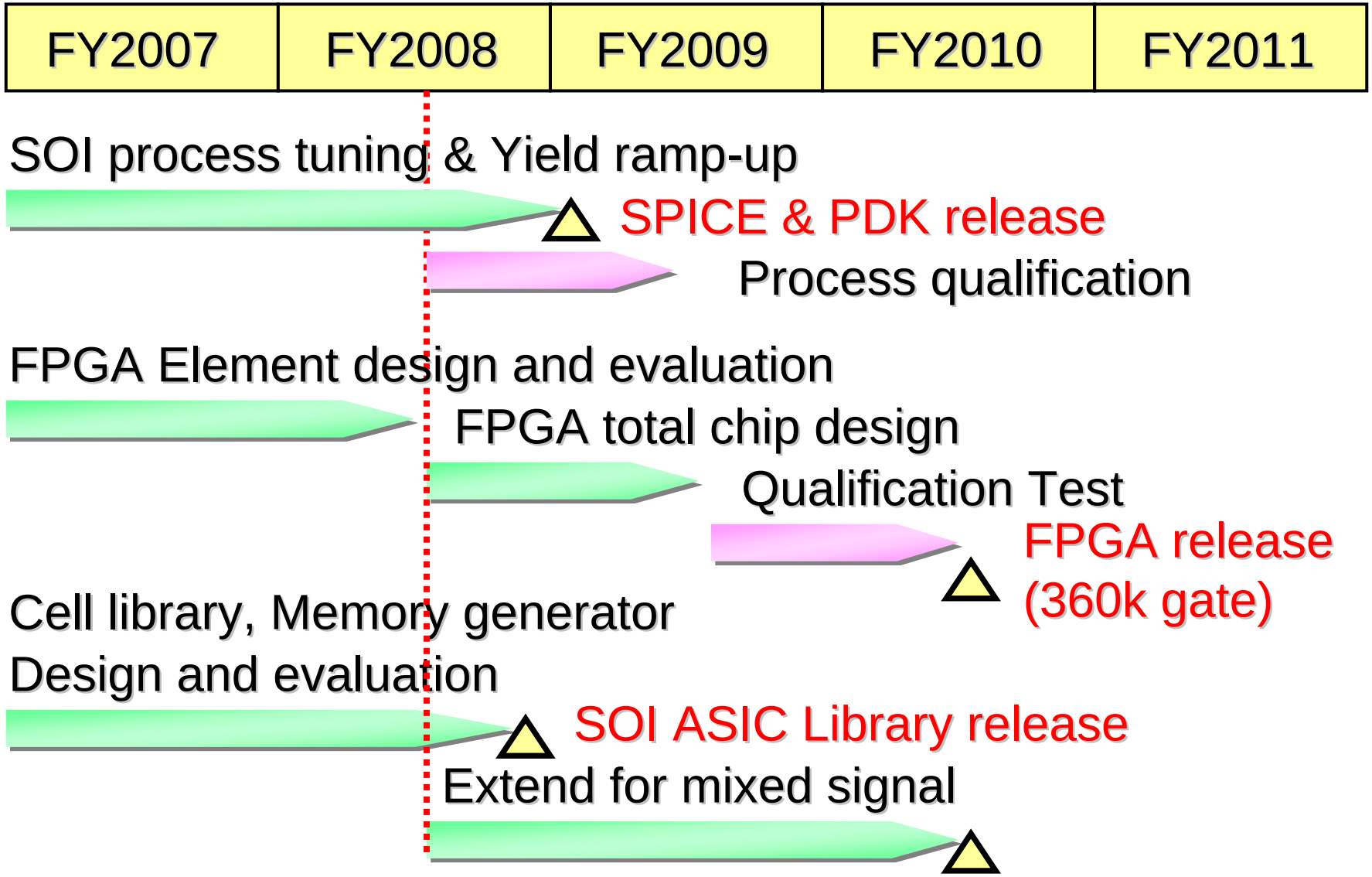
Joint development with CNES / ATMEL

- SRAM based re-configurable FPGA. (Based on ATMEL architecture)
- 360k, 700k, 1M ASIC gates

FPGA

RHBD: Radiation Hardened By Design
TID: Total Ionizing Dose LET: Liner Energy Transfer

Current status for SOI ASIC / FPGA



For the next mission..

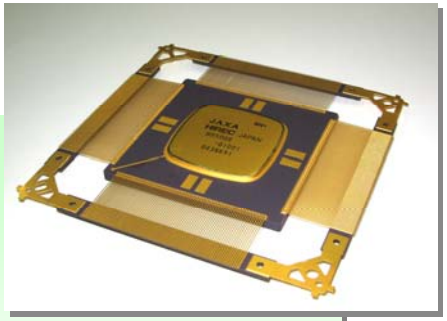
Some scientific satellite programs plan to use current 64bit MPU.

However, future missions request higher tolerance to SEE, higher performance to the next MPU.

SOI technology becomes one of the most suitable solution for next generation.

Improvement of MPU by SOI technology

- 0.18μm CMOS
- 1.8V / 3.3V
- 64bit, 200MHz
- 5W @ 200MHz
- On-chip peripheral
- SEU (LET_{th}):
  logic : >64 [MeV/(mg/cm^2)]
  Cache : 0.46 [MeV/(mg/cm^2)]
- SEL (LET_{th}) :
  >64 [MeV/(mg/cm^2)]



- 0.15μm FD-SOI
- 1.5V / 3.3V
- 64bit, >300MHz (TBD)
- Modified peripheral
- SEU (LET_{th}): (TBD)
  logic : >64 [MeV/(mg/cm^2)]
  Cache :>40 [MeV/(mg/cm^2)]
- SEL : Immune

Improvement of

- SEU tolerance (Cache)
- Function of peripheral
- Speed, Power consumption

Development plan for improved MPU

FY2008	FY2009	FY2010	FY2011	FY2012

Synthesis & layout of current MPU design for SOI.
Improvement of cache memory, exception handler.

Type A*

QT

△ FM release

Specification fix (modified peripheral)

Type B**

Design & evaluation

Synthesis & layout

QT

△ FM release

***Type A : The same design as present MPU (without PLL). Rad-hard cache memory.**
****Type B : MPU with modified on-chip peripheral. Rad-hard cache memory.**

Summary

- For most of the 1st phase items (i.e. MPU, SRAM, Power MOSFET and DC/DC converter), QTs were successfully completed.
- Development of POL, p-ch MOSFET and SOI ASIC / FPGA is in progress.
- Development of Mixed signal SOI ASIC and SOI-MPU will start this fiscal year.
- We would like to accelerate the discussion concerning the candidates for the second phase items including possible collaborations with ESA and CNES.