Qualification and Reliability of Actel RTAX-S Space-Flight FPGAs

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Area Technical Manager
Actel Japan K.K.
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Agenda

- Qualification activities on RTAX-S/SL
  - Overview of designs and data collected
  - QML Class V qualification update
  - NASA and aerospace data

- Quality and reliability
  - Power supply transient (SET) investigation
  - Process flow enhancements
  - Reliability information on failures-in-time (FIT) rates
  - Reports and certifications

- Summary
Qualifications
Per MIL-STD-883G TM5005.14, a series of tests are required to be performed for qualification purposes:

- Class B tested devices
- Program a design
- Pre burn-in parametric and functional verification at 3 temperatures

168, 500 hour pull points with test points
- Burn-in @ 125°C

- Burn-in @ 125°C 1000 hours

- Delta calculations, with end of process steps
- Publish results and get TRB approval
RTAX-S/SL Qualification

- Per MIL-STD-883B, qualification activities were completed in two phases
  - Phase 1 covered RTAX250S/SL, RTAX1000S/SL and RTAX2000S/SL
    - Qualification was completed in 2005
    - DSCC released and certified QML-Q SMDs in April 2006
  - Phase 2 covered RTAX4000S/SL
    - Qualification was completed in 2007
    - DSCC released and certified QML-Q SMDs in August 2009
  - RTAX-S/SL devices can now be ordered to the DSCC SMD “5962” number at: http://www.dscc.dla.mil/Programs/Smcr.
RTAX-S/SL Qualification

Several sets of data with different sets of designs were collected to ensure reliability of RTAX-S/SL devices

- **Qualification burn-in (QBI) design**
  - Targeted for CMOS, feature set and maximum utilization
  - Group A, B, C, D, ESD and I/O capacitance data was collected

- **Enhanced antifuse qualification (EAQ)**
  - Used design with high observability of timing changes to detect weak or misformed antifuses

- **High single S-Antifuse and high single B-Antifuse (HSB) design**
  - Used design with high perceptibility of multiple delay lines
  - Covered maximum utilization of both single S-Antifuse and single B-Antifuse
### RTAX-S/SL Qualification

#### Summary of data collected:

<table>
<thead>
<tr>
<th></th>
<th>RTAX2000S (# units*Hours)</th>
<th>RTAX1000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>QBI</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HTOL</td>
<td>87 *1000</td>
<td>98*1000</td>
<td>185,000</td>
</tr>
<tr>
<td>LTOL</td>
<td>-</td>
<td>78*1000</td>
<td>78,000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>RTAX2000S (# units*Hours)</th>
<th>RTAX1000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EAQ</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HTOL</td>
<td>-</td>
<td>120*6000</td>
<td>720,000</td>
</tr>
<tr>
<td>LTOL</td>
<td>-</td>
<td>120*250</td>
<td>30,000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>RTAX2000S (# units*Hours)</th>
<th>RTAX1000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HSB</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HTOL</td>
<td>-</td>
<td>298*1000</td>
<td>298,000</td>
</tr>
<tr>
<td>LTOL</td>
<td>-</td>
<td>298*250</td>
<td>74,500</td>
</tr>
</tbody>
</table>

HTOL: High Temperature Operating Life (125° C), LTOL: Low Temperature Operating Life (-55° C)
RTAX4000S/SL Qualification

- RTAX4000S was introduced at the end of 2007
  - This is the highest density antifuse device with 4M system gates
  - In addition this device has a unique feature set known as "generic burn-in"
- Qualification was completed using a "master design"
  - This design incorporates the QBI, EAQ, HSB and SEE (for TID) portions into one design
  - Targets CMOS, antifuse and package related qualification activities

<table>
<thead>
<tr>
<th>Master Design</th>
<th>RTAX4000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>77 *1000</td>
<td>77,000</td>
</tr>
<tr>
<td>LTOL</td>
<td>24*250</td>
<td>6000</td>
</tr>
</tbody>
</table>

HTOL : High Temperature Operating Life (125° C), LTOL : Low Temperature Operating Life (-55° C)
RTAX-S Design Overview

- RTAX4000S design utilization
  - Different I/O standards are utilized in the design
    - Single ended, differential and voltage referenced I/Os are configured
  - QBI design
    - Maximum logic cell utilization
    - Test all I/O standards
    - Test all macros offered (carry chain, buffers, etc.)
    - Test RAM feature

<table>
<thead>
<tr>
<th>Info</th>
<th>Utilization</th>
<th>Logic Cells</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Pins</td>
<td>Clocks</td>
<td>seq + combo</td>
</tr>
<tr>
<td>RTAX4000S</td>
<td>CG1272</td>
<td>I/O RCLK HCLK RAM/FIFO Carry Chain R-Cell C-Cell</td>
<td>99.96%</td>
</tr>
<tr>
<td></td>
<td>840</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>
EAQ Design Overview

- High perceptibility of delay measurement deltas
  - Multiple combinatorial delay lines, I/O test block, RAM test blocks

![Diagram of EAQ Design Overview]
HSB Design Overview

- Goal of high single S-Antifuse and single B-Antifuse design
  - Increase the utilization of single S-Antifuse and single B-Antifuse
  - Short delay lines of combinatorial and sequential logic
  - Both sequential and combinatorial delay lines exercised during burn-in with the same 2 MHz clock frequency

Combinatorial delay lines

Sequential delay lines
RTAX4000S/SL Generic Burn-In

- Generic burn-in feature: unique to RTAX4000S/SL
  - Complete network exercise compared to less than 70% AC toggle coverage achieved by ASIC burn-in test vectors
  - No design-specific test patterns needed for any user-programmed RTAX4000S/SL design
  - No specific burn-in boards required to accommodate custom user designs
  - RTAX4000S/SL programmed parts with multiple designs can be burned-in simultaneously using Actel generic burn-in boards
  - The generic burn-in test is implemented using existing global test circuit commands
Simplified Signal Path Schematic

Schematic of the combinatorial module path

By toggling the X3 and Test_SEU control inputs of each “Primary Component” module, the outputs of the secondary modules will toggle. As a result, the network routing driven by that module will be exercised.

All antifuses associated with the normal user circuit path will be exercised.
Verification of the generic burn-in concept was performed with software simulation and burn-in system.

- Bench-level testing using dedicated Silicon Explorer probe pin outputs and TDO outputs verified cell toggling on all the available device features.
- Logging of pre and post burn-in data is required.

Generic burn-in qualification was completed with 1000 HTOL hours.

- Pre and post burn-in data is logged and compared at each pull-point.
- All devices passed successfully with no delay or faults observed.

### Generic Burn-In Verification and Qualification

<table>
<thead>
<tr>
<th>Master Design</th>
<th>RTAX4000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>24 *2000</td>
<td>48,000</td>
</tr>
</tbody>
</table>

HTOL: High Temperature Operating Life (125°C)
RTAX-S Reliability Testing Round-Up

- Aerospace Corporation testing (Axcelerator)
  - Longest running parts > 20,000 HTOL hours
  - >13 Million device hours accumulated!
  - One failure (SRAM) under investigation

<table>
<thead>
<tr>
<th>Type</th>
<th>Devices</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>AX2000 HTOL</td>
<td>277</td>
<td>5,380,545</td>
</tr>
<tr>
<td>AX2000 LTOL</td>
<td>274</td>
<td>4,898,275</td>
</tr>
<tr>
<td>AX2000 Temp Cycle</td>
<td>189</td>
<td>3,219,043</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>13,497,863</strong></td>
</tr>
</tbody>
</table>

- NASA GSFC
  - Testing completed, no anomalies observed to date
  - New aerospace program wants to continue this experiment to 10,000 cumulative hours

<table>
<thead>
<tr>
<th>Type</th>
<th>Devices</th>
<th>Hours</th>
<th>Cumulative Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTAX250S HTOL</td>
<td>82</td>
<td>3000</td>
<td>246,000</td>
</tr>
<tr>
<td>RTAX250S LTOL</td>
<td>82</td>
<td>3000</td>
<td>246,000</td>
</tr>
<tr>
<td>RTAX2000S HTOL</td>
<td>82</td>
<td>3000</td>
<td>246,000</td>
</tr>
<tr>
<td>RTAX2000S LTOL</td>
<td>82</td>
<td>3000</td>
<td>246,000</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td><strong>984,000</strong></td>
</tr>
</tbody>
</table>
RTAX-S Reliability Summary

- No antifuse anomalies observed in testing to date
- Device hours accumulation
  - More than 16 Million device hours accumulated on the 0.15 µm technology including independent testing run by NASA and Aerospace Corp.
  - Greater than 4.5 Million device hours have been accumulated on RTAX-S alone (including ORT data)
- Actel calculates overall product FIT < 10
  - Using the chi-square distribution and a minimum upper confidence limit of 60% per JESD74 and $E_A = 0.7eV$
QML Class V Qualification Update
QML Class V Qualification: RTAX-S/SL

- Qualification vehicle used: RTAX4000S
  - Qualifies all RTAX-S/SL device by extension
    - RTAX250S/SL, RTAX1000S/SL and RTAX2000S/SL
- 77 units were processed through "EV" flow
  - 75 units completed 6000 hours
  - One packaging anomaly at 3000 hour reported, analysis revealed incorrect test condition was used during gross leak test
    - FA report available upon request

<table>
<thead>
<tr>
<th>Master Design</th>
<th>RTAX4000S (# units*Hours)</th>
<th>Total # of Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>75 *6000</td>
<td>450,000</td>
</tr>
<tr>
<td>HTOL</td>
<td>1(Ref unit) *3000</td>
<td>3,000</td>
</tr>
<tr>
<td>HTOL</td>
<td>1</td>
<td>Package Anomaly</td>
</tr>
</tbody>
</table>

HTOL: High Temperature Operating Life (125°C)
Power Supply SET Investigation
Power Supply SET Investigation

- Third-party RH regulators can sometimes exhibit single event transient (SET) effects
  - Output voltage glitches to levels close to the unregulated power supply voltage
  - This is a potential hazard for all devices powered by these regulators (not just FPGAs)
- An investigation was done to study the effects of these glitches on Actel's RT devices
  - Study covered RTAX-S/SL and RTSX-SU devices
AC Stress: RTAX-S/SL

- Devices were programmed with EAQ design
- All tests were done at room temperature
- Both $V_{CCA}$ and $V_{CCI}$ power supplies were stressed
- Clocks were running at 20 MHz during these experiments
- Devices were tested for functional and parametric changes

<table>
<thead>
<tr>
<th>RTAX2000S</th>
<th>Stress Condition</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>26 devices</td>
<td>$1.5 \text{ V} + 2.5 \text{ V} = 4 \text{ V}$</td>
<td>Pass</td>
</tr>
<tr>
<td>26 devices</td>
<td>$3.3 \text{ V} + 2.7 \text{ V} = 6 \text{ V}$</td>
<td>Pass</td>
</tr>
</tbody>
</table>
DC Stress: RTAX-S/SL

- Devices were programmed with EAQ design
- All tests were done at room temperature
- Both $V_{CCA}$ and $V_{CCI}$ power supplies were stressed
- Clocks were running at 20 MHz during these experiments
- Devices were tested for functional and parametric changes

<table>
<thead>
<tr>
<th>RTAX2000S</th>
<th>Stress Condition</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>26 devices</td>
<td>1.5 V (0.1 V incr) $\rightarrow$ 3.5 V</td>
<td>Pass</td>
</tr>
<tr>
<td>26 devices</td>
<td>3 V (0.1 V incr) $\rightarrow$ 5.5 V</td>
<td>Pass</td>
</tr>
</tbody>
</table>
AC Stress: RTSX-SU

- Devices were programmed with ELA design
- All tests were done at room temperature
- $V_{CCA}$ and $V_{CCI}$ power supply was stressed
- Clocks were running at 20 MHz during these experiments
- Devices were tested for functional and parametric changes

<table>
<thead>
<tr>
<th>RTSX72SU</th>
<th>Stress Condition</th>
<th>Stress</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>17 devices</td>
<td>2.5 V + 3 V = 5.5 V</td>
<td>AC</td>
<td>Pass</td>
</tr>
<tr>
<td>17 devices</td>
<td>5 V + 2.5 V = 7.5 V</td>
<td>AC</td>
<td>Pass</td>
</tr>
</tbody>
</table>
DC Stress: RTSX-SU

- Devices were programmed with ELA design
- All tests were done at room temperature
- $V_{CCA}$ and $V_{CCI}$ power supply was stressed
- Clocks were running at 20 MHz during these experiments
- Devices were tested for functional and parametric changes

<table>
<thead>
<tr>
<th>RTSX72SU</th>
<th>Stress Condition</th>
<th>Stress</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>17 devices</td>
<td>2.5 V (0.1 V incr) → 4.5 V</td>
<td>DC</td>
<td>Pass</td>
</tr>
<tr>
<td>17 devices</td>
<td>5 V (0.1 V incr) → 6.5 V</td>
<td>DC</td>
<td>Pass</td>
</tr>
</tbody>
</table>
Summary of SET Investigation

- Devices were stressed beyond their absolute maximum rated conditions using DC and AC stress
- Outcome of the study indicates RTAX-S and RTSX-SU devices are robust and reliable
  - But customers are advised against stressing beyond the conditions outlined in the datasheet
- Datasheet remains unchanged
- Whitepaper outlining the investigation and analysis is planned for external publication
  - Paper was published at MAPLD 2009
  - Actel can share the investigation report upon request
Process Flows and Enhancements
Process Flow Enhancements

- **XY wafer location programming (RTAX-S and RTSX-SU)**
  - Wafer number and die location programmed into each unit during wafer sort
    - Assists with traceability and failure analysis

- **Programming software revision stamping (RTAX-S)**
  - Silicon Sculptor programming SW revision is programmed into device concurrent with customer design programming
    - Assists with traceability and failure analysis

- **Thermal runaway characterization (RTAX-S)**
  - Performed on each wafer lot (started with lots fabricated in 2007)
  - Two samples are programmed with ELA design and current is measured at junction temperature $T_J$ of 140°C, 145°C and 150°C
  - Lots exhibiting thermal runaway at $T_J$ 150°C or lower are scrapped
  - Recommended maximum junction temperature $T_J = 125°C$
  - Absolute maximum junction temperature $T_J = 135°C$
Process Flow Enhancements

- **Antifuse XSEM (RTAX-S and RTSX-SU)**
  - Two dice per wafer are cross-sectioned (XSEM) to assess antifuse form and construction
    - Wafers that meet the criteria are moved to the next set of steps
    - Wafers that do not meet the criteria are scrapped

- **Enhanced lot acceptance test (RTAX-S and RTSX-SU)**
  - Sample of units from each wafer lot are programmed life tested for 168 hours @ 125° C
  - Failure criteria includes functional and parametric limits, and outliers on parametric distributions

- **Enhanced E-test (RTAX-S and RTSX-SU)**
  - Additional E-test sites on all RTSX-SU and RTAX-S wafers are tested after wafers are received in Actel facility
  - Any wafers that do not meet set criteria are scrapped
Certifications
&
Reports
Actel's quality policy is to consistently meet customer expectations by continual improvement of quality and the quality management system (QMS).
Reliability

- Actel performs quarterly on-going reliability tests (ORT)
  - Data in this report includes
    - FIT rates for every product and technology node
    - ESD summary by product family
    - Reliability summary for every node
  - Report can be found at:
    http://www.actel.com/techdocs/qualrel/default.aspx

### Reliability Summary

<table>
<thead>
<tr>
<th>Device Technology</th>
<th>Number of CMOS Failures</th>
<th>Device Hours</th>
<th>T_j(°C)</th>
<th>EA, eV</th>
<th>Confidence</th>
<th>FIT</th>
<th>MTTF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 μm CMOS FPGA</td>
<td>1</td>
<td>3.11E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>6.45</td>
<td>1.54E+08</td>
</tr>
<tr>
<td>1.0 μm CMOS FPGA (RH1020)</td>
<td>0</td>
<td>3.97E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>23.05</td>
<td>4.34E+07</td>
</tr>
<tr>
<td>0.8 μm CMOS FPGA (RH1200)</td>
<td>1</td>
<td>9.19E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>22.04</td>
<td>4.54E+07</td>
</tr>
<tr>
<td>0.8 μm CMOS FPGA</td>
<td>1</td>
<td>1.67E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>5.46</td>
<td>1.83E+08</td>
</tr>
<tr>
<td>0.6 μm CMOS FPGA</td>
<td>0</td>
<td>1.82E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>5.04</td>
<td>1.09E+08</td>
</tr>
<tr>
<td>0.6 μm RT545X CMOS FPGA</td>
<td>0</td>
<td>2.29E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>39.88</td>
<td>2.51E+07</td>
</tr>
<tr>
<td>0.45 μm CMOS FPGA</td>
<td>0</td>
<td>6.95E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>13.16</td>
<td>7.60E+07</td>
</tr>
<tr>
<td>0.35 μm CMOS FPGA</td>
<td>0</td>
<td>6.31E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>14.51</td>
<td>6.89E+07</td>
</tr>
<tr>
<td>0.25 μm MEC CMOS FPGA</td>
<td>2</td>
<td>7.51E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>41.40</td>
<td>2.42E+07</td>
</tr>
<tr>
<td>0.25 μm Infracon Flash CMOS FPGA</td>
<td>0</td>
<td>3.62E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>25.30</td>
<td>3.98E+07</td>
</tr>
<tr>
<td>0.25 μm UMC CMOS FPGA</td>
<td>0</td>
<td>7.26E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>1.26</td>
<td>7.92E+08</td>
</tr>
<tr>
<td>0.22 μm UMC CMOS FPGA</td>
<td>0</td>
<td>4.99E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>1.83</td>
<td>5.45E+08</td>
</tr>
<tr>
<td>0.22 μm Flash CMOS FPGA</td>
<td>0</td>
<td>4.92E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>18.59</td>
<td>5.38E+07</td>
</tr>
<tr>
<td>0.16 μm UMC CMOS FPGA</td>
<td>1</td>
<td>1.80E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>11.23</td>
<td>9.90E+07</td>
</tr>
<tr>
<td>0.13 μm Infracon Flash CMOS FPGA</td>
<td>0</td>
<td>2.49E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>3.68</td>
<td>2.72E+08</td>
</tr>
<tr>
<td>0.13 μm Flash CMOS FPGA</td>
<td>0</td>
<td>7.75E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>11.78</td>
<td>9.55E+07</td>
</tr>
</tbody>
</table>

Note: Please refer to the “Anti-fuse Reliability Overview” on page 34 for RT5X-SU anti-fuse FIT rate reliability data.
Radiation Reports

- Total ionizing dose (TID) reports are published for every wafer lot that is processed at Actel (http://www.actel.com/products/milaero/hireldata.aspx)
- Single Event Upset (SEU) and Single Event Latchup (SEL) reports are published for all RT families (http://www.actel.com/products/milaero/hireldata.aspx)
- Neutron testing covers Actel device immunity to soft and firm errors (http://www.actel.com/products/solutions/ser/)
- Related high reliability whitepapers can be found:
  - RTAX-S Testing and Reliability Update (http://www.actel.com/documents/RTAXS_Rel_Test_WP.pdf)
RTAX-S Now in Space!

- **Cosmo-SkyMed 1, 2, and 3**
  - First Launch June 2007
  - RTAX2000S-CQ352

- **Mars Phoenix**
  - Launched August 2007
  - RTAX1000S-CQ352

- **TWSAT**
  - Launched April 2008
  - RTAX2000S-CQ352

- **Chandrayaan-1**
  - Launched October 2008
  - RTAX2000S-CQ352

- **Sicral-1B**
  - Launched April 2009
  - RTAX2000S-CQ352

- **LRO and LCROSS**
  - Launched June 2009
  - RTAX2000S-CG624
  - RTAX2000S-CQ352
Planning to Fly RTAX-S

<table>
<thead>
<tr>
<th>Satellite</th>
<th>Mission Description</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Galileo</td>
<td></td>
<td>CQ352</td>
</tr>
<tr>
<td>Advanced EHF</td>
<td></td>
<td>CQ352</td>
</tr>
<tr>
<td>NPOESS</td>
<td></td>
<td>CG1152 - 6 Σ</td>
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James Webb Space Telescope
Summary

- Actel RTAX-S/SL FPGA products combine high performance, low power and unprecedented reliability to bring value to Space customers.
- Units are processed to the most stringent requirements per MIL-PRF-38535 and MIL-STD-883G.
- QML Class V certification is in development, expect RTAX-S in 2010.
- Actel is committed to Space customers by continuously improving process flows, improving acceptance criteria and adding new products to the portfolio.