Current status of MPU development for space

Oct. 16th 2009

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(1) On-orbit demonstration result of 320MIPS 64bit MPU (SDS-1 satellite, AMI component)

(2) Current status of MPU development utilizing 0.15um FD-SOI CMOS process
(1) On-orbit demonstration result of 320MIPS
64bit MPU (SDS-1 satellite, AMI component)
Flight demonstration (SDS-1)

1st phase critical parts

AMI

SDS-1 was launched on Jan. 23rd, 2009.

Sun-synchronous orbit, 666km

SDS-1 : Small Demonstration Satellite #1
MIPS64 5kf architecture with on-chip peripherals.
0.18μm commercial CMOS process.
200MHz operation (320MIPS)
JAXA qualified. (Mar. 2007)
### SEU sensitivity of element circuits for 320MIPS 64bit MPU

<table>
<thead>
<tr>
<th></th>
<th>SRAM cell for cache memory</th>
<th>RH-latch for MPU logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>LET&lt;sub&gt;th&lt;/sub&gt; (onset) [MeV/(mg/cm²)]</td>
<td>0.46</td>
<td>&gt; 40.3</td>
</tr>
<tr>
<td>σ&lt;sub&gt;sat&lt;/sub&gt; [cm²/bit]</td>
<td>3.16E-07</td>
<td>&lt; 1.05E-09</td>
</tr>
</tbody>
</table>

- **RHBD** (Radiation Hardened by Design) methodology was **utilized for MPU logic** in order to eliminate SEUs.
- For cache memory, **RHBD was not applied** as a result of trade-offs of operation speed, of the area penalty, etc.
- Specially designed memory configuration and parity check were applied to identify any cache errors.
AMI board configuration

- MPU board
- 320MIPS 64bit MPU
- EEPROM
- RS-422 driver
- FPGA
- B-SRAM
- ADCx9ch
- Over current protection
- 15V to 1.8V
- 15V to 3.3V
- 15V to 5V
- 28V Power supply
- RS-422
- Power supply Board & DC/DC conv.

The 22nd Microelectronics Workshop @ Tsukuba
Two types of programs (Quick sort & FFT) were executed continuously in order to check SEUs.

Error exception handler (designed by JAXA) for cache error identification and for correction was installed.

Depending on the situation, the handler can later resume the execution at the original location using the saved information.

Monitoring items are listed below.
- Number of SEUs
- Time of occurrence
- Logical memory address (BSRAM)
- Cache error register information (MPU)
Exception handler flow

1. Save the register information in the stack area.
2. Specify the category of error.
   (Based on the information on CacheErr register)
3. Identify the location of error.
   (Based on the information on Index)
4. Invalid the corresponding cache line.
   (Correct data is loaded from the main memory.)
5. Calculate the address program is resumed.
   (Based on the information on ErrEPC)
6. Restore the register information.
SDS-1 AMI observation summary

- Total operation time: 593 [hour]
- Number of SEUs observed
  - MPU cache (32kB + 32kB): 3 [events] → 0.12 [events/day]
    - Predicted by CREME96 (without shield): 0.21 [events/day]
  - Burst SRAM (32Mbit): 133 [events] → 5.4 [events/day]
    - Predicted (without shield): 17.5 [events/day]
- All cache errors were correctly detected, and the program returned to the main routine appropriately by the handler.
- Multi-bit SEUs (not in the same word) was observed 8 times for B-SRAM.
Error map of SEUs observed

Observed error data details

MPU cache memory

Detail informations of observed Cache errors

<table>
<thead>
<tr>
<th>Event #</th>
<th>Category of Cache error</th>
<th>Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Instruction cache Data RAM error</td>
<td>0x4770</td>
</tr>
<tr>
<td>2</td>
<td>Instruction cache Data RAM error</td>
<td>0x4788</td>
</tr>
<tr>
<td>3</td>
<td>Instruction cache Tag RAM (Way 1) error</td>
<td>0x3740</td>
</tr>
</tbody>
</table>

MBUs in Burst SRAM

It seems that the same phenomenon (Multi-bit SEUs) which has already been reported in [1] has occurred.

These errors do not become serious problems.
(Not in a word, Correctable.)

(2) Current status of MPU development utilizing 0.15um FD-SOI CMOS process
Some scientific satellite programs plan to use current 64bit MPU.

However, future missions request higher tolerance to SEE, higher performance to the next MPU.

SOI technology becomes one of the most suitable solution for next generation.
Key feature of HR5000S

HR5000S (SOI version of 320MIPS 64bit MPU)

- MIPS64 5kf architecture*.
- \(0.15\mu m\) FD-SOI CMOS process.
- 50MHz operation**
- 304 pin QFP package.
- RHBD techniques is applied to both the logical circuit and the cache memory to improve SEU tolerance.

Logic: >64 [MeV/(mg/cm\(^2\)]
Cache: >40 [MeV/(mg/cm\(^2\)]

*MIPS64 RTL Errata C37 is fixed
**PLL circuit for space use is not available. Now under development.
The main function of the peripheral circuit is equal to 320MIPS 64bit MPU. Modification points are as follows.

- ECC error detection signal output is added to the external signal pins.

- The cache TAG-RAM parity error detection circuit is simplified.

- The terminal that controls the CLKOUT signal is added. Users can select whether the phase of CLKOUT signal is reversed or not.
Development plan for improved MPU

<table>
<thead>
<tr>
<th>JFY2008</th>
<th>JFY2009</th>
<th>JFY2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification fix</td>
<td>Synthesis &amp; layout</td>
<td></td>
</tr>
<tr>
<td>Chip manufacturing</td>
<td>Assembly &amp; evaluation</td>
<td></td>
</tr>
</tbody>
</table>

Current status:
- Synthesis & layout has already been finished.
- Chip manufacturing will be completed this month.

For scientific satellite:
- Such as MMO.

- ES release
- FM release
- QT
- Tape out
The chip size was adjusted to 5mm x 10mm though RHBD was applied to the cache memory. (320MIPS 64bit MPU: 7mm x 10mm)
SDS-1 satellite was launched on this year. The function of the MPU board was successfully demonstrated.

The cache error exception handling mechanism functioned effectively on the orbit.

Development of MPU based on 0.15um FD-SOI technology is in progress. QT will be finished next fiscal year.
Appendix
36M bit burst SRAM for space

- 36Mb, 72(64 data and 8 ECC)-bit x 512k-word
- 100MHz synchronous operation.
- Separated address decoders and cell blocks to prevent multi-bit SEUs in a word.
- The same cell as SRAM used in the MPU cache memory is applied.

Multi chip
(18bit x 512k x 4chip)
AMI component overview

Advanced Micro processing In-orbit experiment equipment

- 200 x 150 x 86 [mm] , 2.3 [kg] , 15[W] (max.)