ASIC, FPGA, ASSPs platforms
Agenda

• ASIC Platform

• ATMX150RHA
  • Features
  • Design Flows
  • ATMEL Analog Cells
  • Partner IP: ISD exemple

• Digital IPs

• Schedule

• Roadmap
Agenda

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• Roadmap
Space Supply Chain
Value added chain

Design Rules
Library Elements
Design Kit
ASSP Expertise

Simulation Files
Test Rules

Simulation Files
Burn-in Conditions
Test Rules

IP Design Flow
Foundry
Probe Test
Assembly
Final Test
Customers

WLA
(Wafer Level Acceptance)
Assembly Rules
Package Drawing
Atmel Aerospace ASIC Platform
Platform Development model for Cost Sharing
180nm, 150nm, 110nm, (90nm), 65nm

Core Platform Design
Rad Hardening
Pre Qualification

Embedded FPGA
RH HW blocks add on
Secured Database
tbd

Core Architecture
Custom

Rad Hardening Technology
Core IPs

Standard Products
Building blocks for ASIC & FPGA

KEY PARTNERS
ASIC & FGA
Customer Specific Design
Cost benefits
IP access
ASIC PLATFORMS

Improving ATMEL Aerospace ASIC offering

Make durable the current digital ATC18RHA ASIC family, switching to an Atmel technology used in qualified automotive business with huge volumes.

Improve integration with versatile technology: a mixed-signal strategy

- Logic
- Analog
- 5V compatibility
- Embedded NVM (EEprom)
- High voltage option
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150nm Technology in 5LM on SOI

- Re-used process module and combined devices construction coming from commercial and Automotive technologies on same nodes
ATMX150RHA

General features

- 150 nm technology
  Up to 7M equivalent NAND2 gates

- Double pad ring, 95µm Pad pitch

- Core supply 1.8V

- I/O's
  - 5, 3.3 & 2.5 V and a HV option (30V - 60V)
  - High Speed LVDS Buffers (655Mbps)
  - PCI Buffers

- A catalog of qualified Analog blocks

- SRAM/DPRAM and NVM blocks

- Standardized Packages but also Dedicated packages
ATMX150RHA

Technology features

• Operating temperature range
  from -55°C to +125°C ambient temperature

• Radiation (target)
  TID > 300 krad(Si)
  SEL : LET > 60 MeV/mg/cm² at 125°C
  SEU/SET: LET > 30 MeV/mg/cm²

• Life time
  20 years at Tj = 110°C
**ATMX150RHA**

The Full Management of your Mixed-signal flow

If customer analog blocks

- Target: Quarterly SMPW to embark test vehicles at low cost
- Atmel offers Probe/assembly/test services
- Qualification services (reliability, TID, SEE…)

If Atmel pre-qualified analog blocks

- Get access to a full qualified catalog
- No more test vehicles
- No more specific qualification tests
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ATMX150RHA

A Design flow depending on ASIC type

Full Digital or ASIC Designed with Atmel analog blocks

- Atmel starting from synthetized netlist
- Atmel manages the manufacturing flow foundry/probe/assembly/test and qualification
- Atmel manages the Package development
- Tools

<table>
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<tr>
<th>Task</th>
<th>CAD provider</th>
<th>Tool</th>
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<tr>
<td>Design Entry</td>
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<td>High Level Synthesis tool</td>
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<td>HDL simulation</td>
<td>Mentor</td>
<td>Questasim</td>
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<td>Design Compiler (topo/graphical)</td>
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<td>DFT insertion</td>
<td>Synopsys</td>
<td>DFT Compiler</td>
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<td>Primetime Suite</td>
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<td>Tetramax</td>
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<td>Top Checks</td>
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ATMEL Qualified Analog blocks

- PLL (multi-range)
- ADC (12 bits)
- DAC (12 bits)
- Multiplexer (4 / 8 channels)
- Oscillators (10 MHz, 45 MHz)
- Comparator
- BandGap reference
- Voltage regulator
- Temperature sensor
ATMX150RHA

PLL - Phase-Locked Loop 40-450 MHz

- Already used in ATC18RHA

- Main features
  - Placement: Periphery
  - Supply: 1.8V
  - Programmable VCO - range from 40MHZ to 450MHz
  - 4 phases VCO outputs (0,90,180,270 degrees)
  - Programmable internal Loop Filter
  - Dedicated 1.8V Power Supply (VCCPLL/VSSPLL)
  - Consumption: Dyn. 7.5mA, (max) ; Stat. 10uA (max)

- Dimensions (hardened)
  - X=250um, Y=552um, Area 0.14mm²

- Number of Pins
  - Total = 21

![Block diagram]

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<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<td>1.8</td>
<td>2.0</td>
<td>V</td>
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<td>450</td>
<td>MHz</td>
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<td>Fout/Fin</td>
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<td>15</td>
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<td>VCO outputs</td>
<td>45</td>
<td>55</td>
<td>%</td>
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<td>VCOPhases</td>
<td>90°/0 or 270°/180°</td>
<td>-5</td>
<td>+5</td>
<td>Deg</td>
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<td></td>
<td>7.6</td>
<td>mA</td>
<td></td>
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<tr>
<td>Idd off</td>
<td>&quot;enplf&quot;l=&quot;0&quot;</td>
<td>10</td>
<td>7.6</td>
<td>uA</td>
<td></td>
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Specification over -55°C to +125°C
ATMX150RHA

ADC - 12bit Cyclic Pipeline ADC (1/2)

- Features
  - Placement: Core
  - Supply: 3.3/1.8V
  - 12-bits Resolution
  - 2MHz Conversion Rate with 32MHz input clock
  - Differential Input Voltage Range 2Vpk-pk
  - Power Down Capability

- Dimensions (not hardened)
  - X=550um, Y=550um

- Number of Pins
  - Total = 35

- ADC 24 bits under discussion with partner
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ADC24 IP Overview

- Discrete time (switched capacitor), 2\textsuperscript{nd} order $\Sigma\Delta$ modulator architecture
- 1 bit internal quantizer
- Sampling frequency: 6kHz – 192kHz (up to 32kHz BW)
- Available in stand-alone (SPI based) and parallel output versions
- Clock frequency 12.288MHz
- Programmable oversampling ratio: x64 – x2048
- Supplies: 1.8V digital core, 3.3V analog and I/Os
- Correlated double sampling for autozeroing and elimination of low frequency (1/f) noise
Dynamic performance

FFT sine 750Hz 3.2Vpp differential input (0dBFS)

![FFT sine wave graph]

117dB SFDR

Reconstructed sine wave at the output of decimator

![Reconstructed sine wave graph]

OpAmp noise PSD

![OpAmp noise PSD graph]

637nV/sqrtHz
OpAmp specifications

Current consumption: 610 uA
Open-loop gain: 76.7 dB
Phase margin: 58 Deg.
Gain margin: -15.5 dB
Bandwidth (-3dB): 22.3 kHz
GPBW: 146 MHz
Slew-rate: 225 V/us
Common mode output: 1.65 V
Current mode input range: 0.35 – 2.95 V
Noise @ 0.1Hz: 640nV/Hz
Die layout

- Test chip of the stand-alone version (SPI)
- Overall chip dimensions: 3000 x 3000 μm
- Cell utilization for the digital core: 0.63
Analog design flow

Architecture & target specifications

Schematic Capture
Virtuoso Schematic Editor XL

PVT simulation
Spectre

Layout
Virtuoso Layout XL

Physical verification
Assura

Cell A

Cell B

Analog top schematic

Analog top Simulation
Spectre

Analog top Layout
Virtuoso Layout XL

LVS/DRC/ERC
Assura

Parasitic extraction
Cadence QRC

Post layout simulation
Spectre

Analog core
DEF Hand-off

CMOS 150nm
AT58K85 5M techno

PDK
Device models

Atmel_fdk_1.0.39_A_
at58850 PDK
LVMOS 3.3V 70A devices

Cadence Virtuoso IC V5.1.41
Custom design flow

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Digital and top design flow

- Synthesis
  - Design Compiler
- Power grid
  - DEF Hand-off
- Analog core
  - DEF Hand-off
- DFT insertion
  - Design Compiler
- Chip-level netlist
  - Digital & Analog core
  - I/O pads
- Place and Route
  - SOC Encounter
- Netlist import
  - Top verilog + Power grid + Analog core
- Standard cell placement
- Clock Tree synthesis (CTS)
- Routing
- Timing verification
- Physical verification
  - (DRC/LVS/ERC)
- Final GDSII
DAC24 IP Overview

- 24-bit resolution
- 3rd order multi-bit ΣΔ modulator architecture
- Adjustable differential current output
- Thermometer coded current source matrix
- Synchronous 24-bit serial input interface with VALID signal
- Selectable oversampling ratios (x32 – x256)
- 1kHz nominal bandwidth
- Nominal sampling frequency 6kHz
DAC24 IP implementation

- 2 cuts of DAC testchip designed, implemented and characterized in CMOS
- Total area 3.42mm²
- Tested up to 100krad TID with no hard-fail or performance degradation
- Design to be ported to Atmel’s AT58K85 150nm techno

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
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<tbody>
<tr>
<td>ENOB</td>
<td>&gt;17 bit (22-bit target)</td>
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<tr>
<td>SNR</td>
<td>130dB</td>
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<tr>
<td>Low freq. Noise</td>
<td>&lt; 10μV/rtHz 10⁴ to 10³ Hz BW</td>
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<td>Linearity</td>
<td>Full code range</td>
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<tr>
<td>Consumption</td>
<td>&lt; 100mW</td>
</tr>
<tr>
<td>TID immunity</td>
<td>&gt; 300krad</td>
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<tr>
<td>LET for SEL immunity</td>
<td>≥ 70 MeV/mg/cm²</td>
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<tr>
<td>SEU immunity</td>
<td>Protection of critical memory cells</td>
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</tbody>
</table>

[Graphs showing PSD](#) Low freq. noise, 0V input and Low freq. noise, DC input
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Examples

One System supported by Atmel

Example of potential deliveries
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ASIC Roadmap

- **65 nm**
  - 30 Mg – 500 MHz

- **90 nm**
  - 15 Mg – 400 MHz

- **180/150 nm**
  - 7 Mg – 300 MHz
  - ATC18RHA
  - Digital customer Mixed-signal
  - ATMX150RHA Mixed-signal – NVM
  - ATMX150RHA with HV

- **350 nm**
  - 3 Mg – 100 MHz
  - MH1RT

Legend:
- FM
- Eng Sample
- Concept

Technology

<table>
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AT65RHA

Developed by STM, deployment by ATMEL with STM support

Features

• 65 nm technology
• Up to 30 usable Mgates equivalent nand2

• Supply voltages: 1.2V for core, 1.8V, 2.5V & 3.3V for I/O’s
• Very low operating consumption
• Compiled memory
• Typical signal I/O’s > 1000 - Flip-Chip technology
• PLL
• Special I/O’s: PCI, HSSL (6.25 Gbps), LVDS (655 Mps)

Expected Radiation Performances

TID: 300Krad
SEL Performances: >95 MeV/mg/cm²