Status of Selected Strategic Projects of the German EEE-Components Qualification Program

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DLR
German Aerospace Center

Aeronautics  Space  Transportation  Energy

- Research Institution
- Space Agency
- Project Management Agency
Locations and Employees

7600 employees across 32 institutes and facilities at 16 sites.


Turnover 3 Billion €
Introduction:

• DLR is taking care of about ten qualification projects each year. Most of these projects run for two years or more.

• Among them we currently regard three projects as strategic ones.

• In particular, we will have a closer look on the following ones:

  ➢ Radiation Characterization of the SG13 Process (130nm Silicon Germanium BiCMOS process)

  ➢ Suitability Examination of a Commercial ASIC Technology for Space Applications and ESCC Capability Approval

  ➢ Qualification of a CCGA (Ceramic Column Grid Array) solder process for Space Applications
Radiation Characterization of the SG13 Process (1)

Why use of SG13 Process?

- Mixed signal possible
- Germanium allows fast structures (up to 120GHz)
- BiCMOS (Bipolar and CMOS structures on same chip) provides good efficiency
- Low to mid volume production possible
Radiation Characterization of the SG13 Process (2)

Goals:

✓ IHP’s SiGe BiCMOS process SG13RH shall be available to the space community for use in space applications and similar environments. (IHP = Innovations for High Performances microelectronics; situated in Frankfurt (Oder), Germany)

✓ Target is both R&D and low- to mid volume production through MPW service and custom mask set production runs.

✓ Suitability to the expected environments shall be demonstrated through a full ESCC evaluation for the manufacturing process.
Radiation Characterization of the SG13 Process (3)

Project Description:

- Assessment of Radiation hardness of IHP’s 130nm SiGe BiCMOS process SG13RH
- Preparation for full ESCC evaluation of the process
  - Design of Test vehicles TCV and DEC for ESCC evaluation
  - Radiation Tests (part of ESCC evaluation procedure)
- Time schedule October 2012 – December 2014
  - TCV radiation tests in Spring/Summer 2014
  - DEC radiation tests in Summer/Fall 2014
Radiation Characterization of the SG13 Process (4)

Challenges (1):

✓ An ESCC Evaluation procedure for mixed-signal technologies does not exist (yet).

✓ ESCC evaluation procedures for silicon devices or microwave devices cover only part of the targeted domain and their requirements are partly contradicting.

✓ Recent research showed degradation in SiGe BiCMOS to be different from Silicon or III/V semiconductors. This is not addressed by any ESCC procedure.
Radiation Characterization of the SG13 Process (5)

Challenges (2):

Both reliability testing and radiation testing pose very different needs on test structures:

- They cannot be served by the same set of devices
- Dedicated devices for radiation testing and reliability testing needed
- Total pad/pin ratio is pretty high compared to usual test vehicles:
  - TCV >100 Pads used (64 pin package)
  - DEC >180 Pads used (128 pin package)
- Maintaining compatibility with standard packages difficult, only possible through variations in bond plan → careful tracking of variants necessary
Radiation Characterization of the SG13 Process (6)

Status:

- TCV manufacturing ongoing, ready by 10/2013
- DEC manufacturing ongoing, ready by 12/2013
- Design of TCV radiation test finished by end of 2013
- Design of DEC radiation test environment started (end spring 2014)
- Preliminary PDK ready, including radhard digital libraries
  - Update when radiation test results are available to include additional simulation corners
  - Expected finalization of PDK by end of 2014
Suitability Examination of a Space ASIC (SPAC) (1)

Why do we need a SPAC?

- Availability of modern, qualified ASIC technology
  - Long-term stable supply of ASICs for space applications
  - Reduced risk of single source dependency
  - Different types of ASICs
  - Suitable for many customers / applications

- Simplified procurement process
  - Reduced effort for qualification
  - One point of contact for customer
  - One company responsible for complete supply chain
Suitability Examination of a Space ASIC (SPAC) (2)

Goals:

✓ Complete supply chain for qualified ASIC

Customer → Manufacturer → Product

- Purchase Order & Specification
- Design & Layout
- Silicon Processing
- Assembly & Test
- Space qualified ASIC
Suitability Examination of a Space ASIC (SPAC) (3)

Project Description:

- Design of test-chip and detailed assessment of the technology
  - Production of test vehicles (wafer processing + packaging)
  - Radiation testing (TID, SEE) & Evaluation

- Definition and development of Space Library
  - Design / development of digital & analog macros
  - Assessment of library elements & definition of Space Library

- ESCC Capability-Approval for the selected domain
  - Create PID + Detail spec
  - Audit

- Evaluation and qualification testing
Suitability Examination of a Space ASIC (SPAC) (4)

Challenges:

- Radiation effects (TID, SEE)
  - Degradation rules
  - Design for radiation hardening required
  - Consideration of Shift in device parameters
  - Radiation tests

- Device reliability
  - Mechanical, functional, parametrical + endurance tests

- Packaging

- Qualification + capability approved domain

- Space Library (further IPs, new library elements)
Suitability Examination of a Space ASIC (SPAC) (5)

Status (1):

- First steps

  - Decision on technology (XP or XH)
  - Definition of macros for test-chip
  - Start of design for test-chip (PETV)
  - Critical Design Review (CDR)
Suitability Examination of a Space ASIC (SPAC) (6)

Status (2):

- Next steps

1. Tape-in test-chip PETV
2. Processing & packaging
3. RVT (TID and SEE) & evaluation
4. Definition of Space Library
Suitability Examination of a Space ASIC (SPAC) (7)

Status (3):

✓ Future steps

- Definition of Space-Library
- Proven rad-hardness of test-chip based on XH-technology

Approval by DLR for start of Phase 2

Successfully passed Capability Approval

Space qualified technology & supply chain for mixed-signal ASIC
Qualification of a CCGA solder process for Space (1)

Why CCGA solder process qualification?

- BGA packages cannot provide sufficient solder quality
- Currently, there is no reliable CCGA solder process with pin count >400 Pins in Europe available
- ICs (i.e. FPGAs) with high pin count are needed parts for space
Qualification of a CCGA solder process for Space (2)

Goals:

✓ Qualification of a CCGA solder process for
  
  • Middle pin count (~600 pins)
  • High pin count (>1000 pins)
  • Very high pin count (>1600 pins)

✓ Develop or select suitable test methods for verification and test

✓ Get a European source for this process: JOP was chosen
  (JOP= Jena Optronik GmbH, situated in Jena, Germany, www.jena-optronik.de)
Qualification of a CCGA solder process for Space (3)

Project Description:

- Development of suitable PCB layout for soldering of
  - Actel CG624 SixSigma
  - Actel CG1272 SixSigma
  - Xilinx CF1752 SixSigma

- Soldering of the samples on the test boards and inspection

- Stress testing (i.e. vibration; temperature cycles)

- Inspection and electrical testing
Qualification of a CCGA solder process for Space (4)

Challenges:

✓ Usage of Virtex 5 technology in space
✓ No official free CCGA process available
✓ Use of ICs with pin count more than 352 pins
✓ Use of automatic soldering instead of hand soldering technology
✓ Evaluate suitable inspection methods
Qualification of a CCGA solder process for Space (5)

Status (1) : What has been done

✓ In deep analysis of the mechanical and thermal behavior of the parts–pcb–frame construct

✓ Investigation of possible inspection methods

✓ Discussion about the layout with the PCB manufacturer Printca Graphics

✓ Assembly of the first boards and visual inspection
Qualification of a CCGA solder process for Space (6)

Status (2) : Future Activities

- Assembly of the 1mm pitch CCGA (1272 / 1752)
- Vibration testing
- 500 thermal cycles -55° C – 100° C and microsection
- 1500 thermal cycles -55° C – 100° C and inspection / electrical test
- Qualification Report
- End of the qualification in Q1/2014
Thank you for your attention!

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Abbreviation list:

• ASIC Application Specific Integrated Circuit
• CMOS Complementary Metal Oxid Semiconductor
• CDR Critical design Review
• DEC Dynamic Evaluation Circuit
• HBT Heterojunction Bipolar Transistor
• MPW Multiproject Wafer Run
• PDK Process Design Kit
• PETV Pre-Evaluation Test Vehicle
• PID Process Identification Document
• RVT Radiation Verification Test
• SEE Single Event Effect
• STI Shallow Trench Isolation
• TCV Technology Characterizing Vehicle
• TID Total Ionizing Dose
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