JAXA Presentation
Wafer Level Chip Scale Packaging (WLCSP)

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Outline

• Purpose for WLCSP

• Insertion point into space applications

• Pros/cons

• Example of a 32 channel multiplexer

• Summary
Purpose of Wafer Level Chip Scale Package

• The introduction of Class Y has opened the door to the use of the non-hermetic packages in space applications
  – Driven highly by the need to access advance technologies that require high density, i.e. FPGAs
  – Additional benefits of small form factor and decrease in weight
  – What about cost? Has not been a driving mechanism, but important.

• Why use a flip chip WLCSP device in space applications?
  – It is a good balance between reliability, small form factor and weight
    • High reliability from a radiation hardened assurance stand point
      – Rad hard by design circuits + total ionizing dose testing + single event effects testing
    • The smallest package available is the die itself
    • Hermetic packages are heavy, made of metals, ceramics and glass
  – What is a good price point?
    • High potential to reduce component cost
Insertion into Space Applications

• From a specification point of view does it make sense for WLCSP be a subset of MIL-PRF-38535 Class Y?
  – Similar to plastic encapsulate microcircuits (PEMs) specification that is being developed and heavily debated today

• What about flight time and heritage?
  – Best application fit now would be for small/nano satellites.
    • Size, weight and cost is driving the use of COTS in some applications
      – WLCSP is good alternative without the need to up-screen
    • Life expectancy of the satellite is relative low

• The gradual progression is toward traditional satellite applications
  – Flight history from nano-satellite applications
    • Overcome the challenges posed by this package
  – Hopefully a specification under class Y that assures reliability
Intersil’s WLCSP Product Selection

• Base die from proven Class V/Q product line
  – TID assurance and SEE characterization

• Wafer level testing of die at 125°C (only)
  – If cold temperature produces a more worst case affect -> 25°C

• Redistribution layer added to die
  – Flip chip mounting directly to the FR-4 PCB
  – RDL designed to ease layout

• Class V die visual inspection
32 Channel Multiplexer Concept Design

- **WLCSP dimensions and features**
  - 5000µm x 4080µm die size
  - 9 x 7 ball grid array with 0.5mm pitch
  - 3 dummy bumps in corners
    - Improves board level reliability i.e. shock and vibration
  - No grid array in center of package
    - Eases PCB layout task
    - Reduces PCB cost and increase reliability
      - No vias under pad or blind and buried vias
  - Board area saving compared to a packaged device
    - Do not forget to include the leads or solder pad openings
32 Channel Multiplexer Concept Design

• **WLCSP size reduction example**
  – 5000μm x 4080μm die size = 20.4 mm²
  – Package device is 14.5 x 14.5 mm = 210 mm²
    - Does not include lead forming → 272 mm²

  – Estimate a satellite uses 20 multiplexers
    - Total board area for WLCSP = 408 mm²
    - Total board area for packaged device = 5440 mm²

  – Board savings estimate
    - $\frac{5440 - 408}{5440} = 92.5\%$

  – WLCSP occupies less than 8% of the board area taken up by the packaged device
Let the Discussion Begin!