150nm process
Mixed-Signal

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Atmel Aerospace

A long history in space

- **1985**  Delivery of the first space product
- **1985 / 1999**  Continuous space product delivery according ESA SCC 9000
- **1999**  US QML qualification by DSCC/DLA
- **1999 – today**  Space product delivery according ESCC 9000 or Mil Prf 38535
- **2000**  RHA qualification by DSCC/DLA
- **2006**  0.35/MH1RT process is ESCC-QML qualified
- **2012**  0.18/ATC18RHA process is ESCC-QML qualified
Atmel Aerospace

Space is our business

• Strong involvement in Space market for more than 30 years with a product offering that matches the needs of the space community

• Recognized and qualified by space agencies

• Space products designed/processed to be radiation-hardened

• All products manufactured according to the latest revision of the ESCC 9000 or MIL PRF-38535

• Atmel Aerospace is a business unit within Atmel that is dedicated to space and HiRel products
Atmel Aerospace

Mission Statement

• High-reliability radiation-hardened products
  • Screening and qualification according to Mil-Prf 38535 and/or ESCC9000
  • Full military operating temperature range (-55 to + 125°C)

• High-reliability products for avionics and defense

• The most advanced technical and competitive solutions
  • Processors (32-bit SPARC)
  • Memories (Up to 16Mb)
  • Communication ICs
  • SRAM-based Reprogrammable FPGAs
  • ASICs (up to 5M gates)
Atmel Aerospace
We are present in all space crafts

• **Transportation**: Ariane 5, ATV, VEGA

• **Earth observation**: Spot 5/Helios 2, Meteosat, MSG, Metop, ERS, Envisat, TeraSar, Sarlupe, Cosmo, Pleiade,

• **Communication**: Argos, Worldstar, Globalstar1&2, Inmarsat, Alphasat,

• **Scientific**: Cassini/Huygens, Hubble, Rosetta, Cluster, Smart-1, Mars Missions, Herschel-Planck, Cryosat, GOCE, Curiosity

• **Navigation**: Galileo
Atmel Aerospace
Qualified R&D and Manufacturing Sites

• **R&D and ASIC development**
  • Atmel France (R&D) and European design centers (ASIC)

• **Wafer fabrication**
  • UMC Taiwan

• **Assembly**
  • E2V Grenoble, France
  • HCM La Rochelle, France

• **Test**
  • Atmel Nantes, France
Space Supply Chain Roadmap

- Extend ATMX150RHA with more MGates capability.
- ATMEL is a leader WW for MPU/MCU using AVR and ARM cores.
- These processes have been funded by CNES and ESA.
Aerospace Value Added
Space/Aerospace Supply Chain

Design Rules
Library Elements
Design Kit
ASSP Expertise
Simulation Files
Test Rules
Simulation Files
Burn-in Conditions
Test Rules

IP Design Flow
Foundry
Probe Test
Assembly
Final Test
Customers
WLA (Wafer Level Acceptance)
Assembly Rules
Package Drawing

ASIC
Standard ASIC
Joined ASSP
end user proprietary
add ASIC to ATMEL catalog
develop the product in partnership with end users
ASIC PLATFORMS

Improving ATMEL Aerospace ASIC offering

Make durable the current digital ATC18RHA ASIC family, switching to an Atmel technology used in qualified automotive business with huge volumes.

Process developed by ATMEL and install at UMC

Improve integration with versatile technology: a mixed-signal strategy

- Logic
- Analog
- 5V compatibility
- Embedded NVM
- High voltage option
ATMX150RHA

General features

• 150 nm technology
  Up to 15M equivalent NAND2 gates

• Double pad ring, 95µm Pad pitch

• Core supply 1.8V

• I/O’s
  o 5, 3.3 & 2.5 V and a HV option (25-45-65V)
  o High Speed LVDS Buffers (655Mbps)
  o PCI Buffers

• A catalog of qualified Analog blocks

• SRAM/DPRAM and NVM blocks

• Standardized Packages but also Dedicated packages
ATMX150RHA

Technology features

• Operating temperature range
  from -55°C to +125°C ambient temperature

• Radiation (target)
  TID > 300 krad(Si)
  SEL : LET > 60 MeV/mg/cm² at 125°C
  SEU on hardened DFF: LET > 30 MeV/mg/cm²

• Life time
  20 years at Tj = 110°C
Context and motivations

- Heavy ions induced Single Event Latchup (SEL) in CMOS devices

- The SEL sensitivity depends on the process, the layout, the power supply and the temperature

- Hardening solutions investigated:
  - Adding Deep wells
  - Adding Deep Trench

> No area cost for deep wells option versus Deep Trench

*Goal: assess by TCAD simulations, the deep Nwell option against the SEL effect*
SEL Hardening solution

- Adding Deep wells
  - Noise reduction of the substrate (by SOI and deep Wells)
  - High reduction of the parasitics PNP & NPN base resistance
  - Reduction of the bipolar gain currents $\beta_{nnp}$ and $\beta_{pnp}$

Standard (without deep wells)

With deep wells:
the Thyristor is not triggered
Devices

Without deepNwell

With DeepNwell
Heavy ion induced SEL

Ion impact: normal incidence in the Nwell/Pwell junction – LET = 80MeV.cm²/mg

Without DeepNwell
- Vcc = 1.98V
- 145°C

=> SEL

With DeepNwell
- Vcc = 1.98V
- 145°C

=> NO SEL
ATMX150RHA

The Full Management of your Mixed-signal flow

**If customer analog blocks**

- Quaterly SMPW to embark test vehicles at low cost
- Atmel offers Probe/assembly/test services
- Qualification services (reliability, TID, SEE...)

**If Atmel pre-qualified analog blocks**

- Get access to a full qualified catalog
- No more test vehicles
- No more specific qualification tests
The Full Management of your Mixed-signal flow

- Design
- Layout
- Manufacturing
- Assembly
- Electrical test
- Radiation
- Screening
- Qualification

With Atmel global management, experience and volumes, customer get

- Pricing stability
- Time saving
- Risk mitigation
ATMX150RHA

A Design flow depending on ASIC type

Full analog

- PDK and DK provided to customer
- Atmel starting from GDSII
- With services of foundry/probe/assembly/test
- With services of qualification
- With management of package development

Tools

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<th>CAD provider</th>
<th>Tool</th>
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<td>Cadence</td>
<td>Virtuoso Schematic Editor</td>
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<td>Analog Simulation</td>
<td>Cadence</td>
<td>MMSIM / AMS</td>
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<tr>
<td>Analog Simulation</td>
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<td>Extraction</td>
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<td>Analog Module Layout</td>
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<td>Top Layout</td>
<td>Cadence</td>
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<tr>
<td>Top Cheks</td>
<td>Mentor</td>
<td>Calibre</td>
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</tbody>
</table>
A Design flow depending on ASIC type

Full Digital or ASIC Designed with Atmel analog blocks

- Atmel starting from synthetized netlist
- Atmel manages the manufacturing flow foundry/probe/assembly/test and qualification
- Atmel manages the Package development

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<td>Design Entry</td>
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<td>High Level Synthesis tool</td>
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<td>HDL simulation</td>
<td>Mentor</td>
<td>Questasim</td>
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<tr>
<td>HDL synthesis</td>
<td>Synopsys</td>
<td>Design Compiler (topo/graphical)</td>
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<tr>
<td>DFT insertion</td>
<td>Synopsys</td>
<td>DFT Compiler</td>
</tr>
<tr>
<td>Memory BIST insertion</td>
<td>Mentor</td>
<td>Tessent MemoryBIST</td>
</tr>
<tr>
<td>P&amp;R, Clock Tree, Crosstalk</td>
<td>Cadence</td>
<td>Encounter</td>
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<td>Cross Talk</td>
<td>Cadence</td>
<td>Celtic</td>
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<tr>
<td>IR drop</td>
<td>Ansys/Apache</td>
<td>Redhawk</td>
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<tr>
<td>Extraction</td>
<td>Synopsys</td>
<td>Star RCXT</td>
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<td>Formal Verification</td>
<td>Synopsys</td>
<td>Formality</td>
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<td>Static Timing Analysys</td>
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<td>ATPG</td>
<td>Synopsys</td>
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<tr>
<td>Post Layout Simulation</td>
<td>Mentor</td>
<td>Questasim</td>
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<td>Calibre</td>
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</table>
A Design flow depending on ASIC type

Analog-on-top & Digital-on-top

- PDK and DK provided to customer
- Atmel manages the digital part (P&R, verifications, Cross-talk, IR drop, parasitics extractions...).
- Analog on top, Digital .LEF provided to customer for top-layout.
- Digital on top, Analog .LEF provided to Atmel for P&R.
- Atmel manages the manufacturing flow foundry/probe/assembly/test and qualification
- Atmel manages the Package development
ATMEL Qualified Analog blocks

- PLL (multi-range)
- ADC (12 bits & 24 bits)
- DAC (10 bits & 24 bits)
- Multiplexer (4 / 8 channels)
- Oscillators (10 MHz, 45 MHz)
- Comparator
- BandGap reference
- Voltage regulator 1.8/5V
- DLL
ATMX150RHA

PLL - Phase-Locked Loop 40-450 MHz

- Already used in ATC18RHA

- Main features
  - Placement: Periphery
  - Supply: 1.8V
  - Programmable VCO - range from 40MHz to 450MHz
  - 4 phases VCO outputs (0, 90, 180, 270 degrees)
  - Programmable internal Loop Filter
  - Dedicated 1.8V Power Supply (VCCPLL/VSSPLL)
  - Consumption: Dyn. 7.5mA, (max); Stat. 10uA (max)

- Dimensions (hardened)
  - X=250um, Y=552um, Area 0.14mm²

- Number of Pins
  - Total = 21

Specification over -55°C to +125°C
ATMX150RHA

ADC - 12bit Cyclic Pipeline ADC (1/2)

• Features
  • Placement: Core
  • Supply: 3.3/1.8V
  • 12-bits Resolution
  • 2MHz Conversion Rate with 32MHz input clock
  • Differential Input Voltage Range 2Vpk-pk
  • Power Down Capability
  • INL +/- 1 LSB
  • DNL +/- 0.5 LSB
  • SNR 70 dB

• Dimensions
  • X=700um, Y=700um

• Number of Pins
  • Total = 35
ATMX150RHA

ADC 24 bits

- 24-bit resolution
- Single-bit ΣΔ modulator topology
- ΣΔ modulator can be combined with external DSP core
- Simple synchronous serial output interface
- Selectable oversampling ratios allow sampling rates up to 96kSa/s
- Analog bandwidth from DC to 16 KHz
- Radiation hardened against SEE and TID
ATMX150RHA

DAC – 10 bits Digital to Analog Converter

• Features
  • Placement: Core
  • Supply: 1.8/3.3V
  • Current dissipation 8mA
  • Resolution: 10-BIT, 15 MHz
  • INL: 0.5 LSB
  • DNL: 0.5 LSB
  • Standby to Active Delay: 40 µs

• Dimensions
  • X=800um, Y=600um

Block diagram
ATMX150RHA

DAC 24 bits

- 24-bit DAC including two DAC cells (main and redundant)
- <70 mW power consumption
- Sampling frequency up to 2 MSa/s
- Bandwidth DC to 330 kHz
- Selectable oversampling ratio
- Multi-bit Sigma-Delta modulator
- >100 krad Total Dose immunity
ATMX150RHA

OSCILLATOR - 10MHz trimmable RC Oscillator

• Main features
  • Placement : core
  • No external components
  • Supply: 1.8V
  • Power consumption 160µA @ 10MHz, 0.2µA standby
  • 10MHz typical frequency clock signal
  • Frequency +/-5 % by using the 7 trimming bits.
  • Stabilizing time 5µs
  • 1.8V Power Supply

• Dimensions
  • X=200um, Y=400um

• Number of Pins
  • Total = 11
ATMX150RHA

OSCILLATOR – 45 MHz trimmable RC Oscillator

• Main features
  • Placement: core
  • No external components
  • Supply: 1.8V
  • Power consumption < 600 μA @45MHz, 1μA standby
  • 45MHz typical frequency clock signal
  • Frequency +/-10% by using the 5 trimming bits.
  • Stabilizing time 10 μs
  • 1.8V Power Supply

• Dimensions
  • X=400um, Y=200um

Block diagram
ATMX150RHA

Analog voltage comparator

• Features
  • Placement: Periphery
  • Supply: 3.3V
  • Vhyst: 500 mV @ 3.3V
  • Consumption
    • Analog mode: 30 μA @ 1MHz
    • Digital mode: 20 μA @ 1MHz, 1pF load
    • Standby: 1μA

• Dimensions
  • X=250um, Y=600um

• Number of Pins
  • Total = 10 (6 I/O + 4 Sup.)
ATMX150RHA

Low Power Bandgap voltage reference

• Features
  • Placement : Periphery/Core
  • Supply: 3.3V
  • Output voltage : (1.21V/1.23V/1.26V)
  • Consumption
    • Dyn. 10 uA
    • Stat. 1uA
  • Temperature coefficient 50ppm/°C
  • PSSR
    • DC to 100Hz : 40dB
    • 10KHz to 100Khz : 5 dB

• Dimensions
  • X=300 um, Y=650um

• Number of Pins
  • Total = 3 (1 + 2 Sup.)
ATMX150RHA

Multiplexer

• Features
  • Placement: Core
  • Supply: 3.3/1.8V
  • 8 channels
  • $R_{ON}$ 250 Ω
  • Analog bandwidth 10MHz
  • Cross talk > 60dB @1MHz

• Dimensions
  • $X=700\text{um}$, $Y=150\text{um}$
Analog IPs Library

Regulator (5V → 1.8V)

• Features
  • Placement: Core
  • Supply: 5V down to 2.5V
  • LDO 700mV
  • Delivering 1.8V @50mA

• Dimensions
  • X=750um, Y=750um
### ATMX150RHA DLL

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f&lt;sub&gt;n&lt;/sub&gt; (1)</td>
<td>Clock frequency</td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td>MHz</td>
</tr>
<tr>
<td>t&lt;sub&gt;DC&lt;/sub&gt; (2)</td>
<td>Delay Cell delay range</td>
<td>0.25</td>
<td>1.35</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>f&lt;sub&gt;DL&lt;/sub&gt; (2)</td>
<td>Delay Line delay range</td>
<td>2 delay cells</td>
<td>0.5</td>
<td>2.7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 delay cells</td>
<td>1.25</td>
<td>6.75</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes:**
1. This is an indicative frequency range. Other operating frequencies can be provided upon request.
2. The delay range values can be adapted to suit the needs of a particular application.

![Diagram of DLL01](image-url)
ATMX150RHA

Radiation results

- **TID**
  - Tested up to 300 krad(Si) + Anneal RT and 100°C
  - 100 krad(Si) - RHA-R level

- **SEU level equivalent to ATC18RHA**
  - LET threshold on Hardened cells at 30 MeV.cm²/mg

- **SEL sensitivity encountered on memory blocks**
  - SEL immunity tested >60 MeV.cm²/mg on Dwell Option (78 MeV)
  - SEL free on Deep Trench Option (N/P isolation)
SEU on SRAM Memories

![Graph showing SEU cross-section vs LET for different SRAM memories, with data points for s/n1, s/n2, and s/n4, and with and without ECC.]
ASIC’s FLIGHT HERITAGE

30-year experience ...

- Globalstar 1998
- Iridium 1998
- Galileo 2011
- Ariane 4/5 From 2008
- Sentinel(s)
- Meteosat/MSG
- Spot(s)
- Space Bus (s)
- Iridiem next 2015
- Rosetta 2004
- Pleiades 2011
- Envisat 2002
- Globalstar 2 Octobre 2010
- Cassini Huygens 1997
- Gokturk 2013