Miniaturation and High-Density Technologies of PCB for space applications

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1. Miniaturization and High-Density Technologies of PCB
2. JAXA-QTS-2140 Appendix G
3. Fine pattern of Inner Layers
4. Small diameter Via hole
5. Via-in-Pad structure / Via Fill
6. Half-Etching of Outer Layers
7. Result of Qualification Test
8. Notice
9. Summary
1. Miniaturization and High-Density Technologies of PCB

- Lead
- Layer 2 signal
- Layer 1 signal

- QFP
- Land

- Half Etching of Outer Layers
- Fine Pattern of Inner Layers

- BGA
- Solder ball

- Layer 1 signal
- Layer 2 signal
- Layer 3 signal
- Layer 4 signal
- Layer 5 signal

- Via-in-Pad Structure
- Small diameter via hole
2. JAXA-QTS-2140 APPENDIX G

Specification of JAXA-QTS-2140 APPENDIX G

Qualified: January 2014

<table>
<thead>
<tr>
<th>Item</th>
<th>Appendix G</th>
<th>Appendix B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Pitch</td>
<td>1.0mm</td>
<td>1.27mm</td>
</tr>
<tr>
<td>Structure</td>
<td>Dog-Bone</td>
<td>Via-in-Pad(VIP) Dog-Bone</td>
</tr>
<tr>
<td>Via Drilled hole Diameter</td>
<td>0.20mm</td>
<td>0.35</td>
</tr>
<tr>
<td>Land Diameter</td>
<td>0.45mm</td>
<td>1.0</td>
</tr>
<tr>
<td>Conductor Width (External)</td>
<td>0.10mm</td>
<td>0.13</td>
</tr>
<tr>
<td>Space</td>
<td>0.15mm</td>
<td>0.18</td>
</tr>
<tr>
<td>Conductor Width (Internal)</td>
<td>0.08mm</td>
<td>0.13</td>
</tr>
<tr>
<td>Space</td>
<td>0.08mm</td>
<td>0.18</td>
</tr>
<tr>
<td>Layer Total</td>
<td>14</td>
<td>16</td>
</tr>
<tr>
<td>Numbers Blind via</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>Maximum Board Thickness Modified Polyimide</td>
<td>2.1mm</td>
<td>2.4</td>
</tr>
<tr>
<td>Low-Z CTE FR-4</td>
<td>2.3mm</td>
<td></td>
</tr>
<tr>
<td>Surface finish</td>
<td>HASL</td>
<td>HASL</td>
</tr>
</tbody>
</table>
Construction

Figure of Cross-section

Blind via hole
Drilled hole diameter = 0.2mm

1.0mm

Layer 1 to 6
= 0.9mm

Layer 1 to 14
Modified Polyimide = 2.1mm
Low-Z CTE FR-4 = 2.3mm

Via hole
Drilled hole diameter = 0.2mm

Conductor width = 0.08mm
Conductor Space = 0.08mm
Example of Pad design

**Dog-Bone**
- BGA
- Blind via
- PTH
- 0.45mm
- 0.65mm

**Via-in-Pad**
- BGA
- Blind via
- PTH
- 0.45mm
- 0.70mm
Design rule of inner layer for 1.0mm pitch via hole.

**Design rule of Appendix G**
- Conductor Width = 0.08mm
- Land Diameter = 0.45mm
- Conductor Spacing = 0.08mm
- Land to Conductor spacing = 0.155mm
- Via hole Diameter = 0.20mm
- Pitch of via hole = 1.0mm

**Design rule of Appendix B**
- Conductor width = 0.13mm
- Land Diameter = 0.75mm
- Land to Conductor Spacing = 0.195mm
- Via Drill Diameter = 0.35mm
- Pitch = 1.27mm

2. JAXA-QTS-2140 APPENDIX G
Example of pattern design:

On these 4 signal layers, lines can be drawn from the pins up to the 9th row.

This design rule enables 1296 pins (Signal 896 pins) mount on BGA/CGA package.
3. Fine Pattern of Inner layers

Cross-section of Patterning for Dry film resist

- UV Lamp
- Work film
- Dry film resist
- Copper Foil
- Base material
- Contact exposure

UV Laser

Laser direct imaging

Exposure + Film = Laser direct imager
4. Small diameter Via hole

<table>
<thead>
<tr>
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<th>Appendix G</th>
<th>Appendix B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Thickness</td>
<td>2.3mm</td>
<td>2.4mm</td>
</tr>
<tr>
<td>Drilled Hole Diameter</td>
<td>0.2mm</td>
<td>0.35mm</td>
</tr>
<tr>
<td>Aspect Ratio</td>
<td>11.5</td>
<td>6.9</td>
</tr>
</tbody>
</table>

Drilling Technology
- High speed rotation Drilling
- Optimization of Drill bits

Plating Technology
- High throwing Power Plating
We select the roll coater in vacuum chamber system for void less via fill.
6. Half-Etching of Outer Layers

Half-Etching equipment

- Half-Etching
- Blind Via hole Plating
- Copper Foil
- Base Material After lamination
- PTH Plating
- Patterning

Patterning Process of Appendix B

- 0.13mm

Patterning Process of Appendix G

- 0.10mm
7. Result of Qualification Test

Sample board over view

- Dog-Bone
- Via-in-Pad
- Dog-Bone
- Via-in-Pad

- Insulation Resistance test coupon (Layer to Layer)
- Conductor (Inner layer)
- Blind via hole
- PTH
- PTH (0.8mm dia.)
- Insulation Resistance test coupons (Inner layer)
We passed the Qualification Test under JAXA-QTS-2140 Appendix G.

The main items of QT are as follows;

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirements</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal shock</td>
<td>-30 to +125 °C, 1,000 cycles (Preconditioning: 240 °C, max. reflow 3 times)</td>
<td>pass</td>
</tr>
<tr>
<td>Solder bath float</td>
<td>288 °C, 10 seconds, 3 times</td>
<td>pass</td>
</tr>
<tr>
<td>Hot oil dip Resistance</td>
<td>260°C, 10 seconds, 10 cycles</td>
<td>pass</td>
</tr>
<tr>
<td>Humidity and Insulation Resistance</td>
<td>25 to 65°C, 90~98%RH, less than 500M ohm</td>
<td>pass</td>
</tr>
<tr>
<td>Dielectric Withstanding Voltage</td>
<td>500Vdc, 30 seconds</td>
<td>pass</td>
</tr>
<tr>
<td>Radiation Hardness</td>
<td>10kGy, less than 500M ohm</td>
<td>pass</td>
</tr>
</tbody>
</table>
7. Result of Qualification Test

7.1 Thermal Shock : Preconditioning

As a preconditioning before Thermal shock test, reflow was performed three times based on JERG-0-043.

<table>
<thead>
<tr>
<th></th>
<th>JERG-0-043 Requirement</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preheat</td>
<td>150+/-10°C 60+/-30sec.</td>
<td>150+/-10°C 81-89sec.</td>
</tr>
<tr>
<td>Reflow</td>
<td>Over 200°C 30-60sec.</td>
<td>Over 200°C 50-65sec.</td>
</tr>
<tr>
<td></td>
<td>Peak temp. Less than 240°C</td>
<td>Peak temp. 231-234℃</td>
</tr>
</tbody>
</table>

Temperature profile
7. Result of Qualification Test

7.1 Thermal Shock : Result of PTH (n=576holes x 4)

The Change in connection resistance

-30°C ⇔ +125°C

Modified Polyimide Max.
Modified Polyimide Min.
Modified Polyimide Ave.
Low Z-CTE FR-4 Max.
Low Z-CTE FR-4 Min.
Low Z-CTE FR-4 Ave.
7. Result of Qualification Test

7.1 Thermal Shock : Result of Blind via (n=576holes x 8)

The Change in connection resistance

-30°C ⇔ +125°C

Graph showing the change in connection resistance over various cycles, with the following lines:
- Modified Polyimide Max.
- Modified Polyimide Min.
- Modified Polyimide Ave.
- Low Z-CTE FR-4 Max.
- Low Z-CTE FR-4 Min.
- Low Z-CTE FR-4 Ave.
7. Result of Qualification Test

7.1 Thermal Shock: Result of Conductor width 0.08mm (n= 4)

The Change in connection resistance

-30°C ⇔ +125°C
7. Result of Qualification Test

7.2 Solder bath float:

288°C x 10sec x 3 times for 0.8mm diameter of PTH(n=12)

Modified Polyimide

Connection of plating and inner layer

Low Z-CTE FR-4
7. Result of Qualification Test

7.2 Solder bath float:

288°C x 10sec x 3 time for 0.2mm diameter PTH(n=15)
7. Result of Qualification Test

7.3 Hot oil dip

Room temperature ⇔ 260°C, 10sec, 10 times
The Change in conductor resistance: under 10%

<table>
<thead>
<tr>
<th>Item</th>
<th>Modified Polyimide</th>
<th>Low Z-CTE FR-4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Average</td>
<td>Max.</td>
</tr>
<tr>
<td>Blind via</td>
<td>-0.2</td>
<td>-0.1</td>
</tr>
<tr>
<td>PTH</td>
<td>-0.3</td>
<td>-0.2</td>
</tr>
<tr>
<td>Conductor</td>
<td>0.9</td>
<td>0.9</td>
</tr>
</tbody>
</table>

Blind via : n=576X8, PTH : n=576x4, Conductor : n=2
7. Result of Qualification Test

7.4 Humidity and Insulation Resistance

25⇌65°C, 90-98%RH, 10cycle.

Requirement of Insulation Resistance: \( \geq 500\,\text{MΩ} (5.00\times10^8\,\Omega) \).

<table>
<thead>
<tr>
<th>Item</th>
<th>Number</th>
<th>Modified Polyimide</th>
<th>Low Z-CTE FR-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer to Layer</td>
<td>14</td>
<td>8.95E+10 Ω</td>
<td>5.09E+11 Ω</td>
</tr>
<tr>
<td>Conductor to Conductor</td>
<td>13</td>
<td>1.98E+11 Ω</td>
<td>4.74E+11 Ω</td>
</tr>
<tr>
<td>Conductor to Blind via</td>
<td>24</td>
<td>6.41E+10 Ω</td>
<td>1.09E+11 Ω</td>
</tr>
<tr>
<td>Conductor to PTH</td>
<td>16</td>
<td>6.32E+10 Ω</td>
<td>1.36E+11 Ω</td>
</tr>
</tbody>
</table>
7. Result of Qualification Test

7.5 Radiation Hardness

Co-60 gamma ray: 10kGy

Requirement of Insulation Resistance: $\geq 500\text{M}\Omega (5.00E+8\Omega)$.

Insulation Resistance of After Irradiation

<table>
<thead>
<tr>
<th>Item</th>
<th>Number</th>
<th>Modified Polyimide</th>
<th>Low Z-CTE FR-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer to Layer</td>
<td>14</td>
<td>1.07E+12 $\Omega$</td>
<td>4.42E+11 $\Omega$</td>
</tr>
<tr>
<td>Conductor to Conductor</td>
<td>13</td>
<td>2.06E+10 $\Omega$</td>
<td>2.10E+11 $\Omega$</td>
</tr>
<tr>
<td>Conductor to Blind via</td>
<td>24</td>
<td>6.43E+10 $\Omega$</td>
<td>3.38E+11 $\Omega$</td>
</tr>
<tr>
<td>Conductor to PTH</td>
<td>16</td>
<td>1.32E+10 $\Omega$</td>
<td>1.54E+11 $\Omega$</td>
</tr>
</tbody>
</table>
Via-in-Pad Structure can be use for soldering BGA/CGA Pad only.
We are considering rectangular Via-in-Pad for mounting rectangular chip parts in the future.
9. Summary

- Miniaturization and High-Density Technologies of PCB needs Fine pattern, Small diameter via hole, Via fill and Half Etching.

- Reliability, miniaturization and high-density of PCBs are realized by using these technologies as shown in JAXA-QTS-2140 Appendix G.
Thank you for your attention.

Mt. Fuji was registered as World Heritage site last year. This is a view from Yamanashi prefecture.