Wrap up of
The 27th Microelectronics Workshop

Component Miniaturization
and
High-Density Technologies
in Space Applications

October 24, 2014
Summary of MEWS 27

Presentation : 28
Attendee : 272

Keywords
Parts level : ASIC / ClassY / SoC / MCM
Non space parts application
Assembly level : CCGA / BGA / CSP / FC
New PCB

New technology : Wireless
Trend of Space Application

Miniaturation, high density, high performance and high efficiency are required for next generation space application.

- High Performance, High Functionality
- High Accuracy
- Multiple Functions
- High-Density
- Miniaturization
- High-Capacity
- Speeding Up
- Low Power Consumption
- Low-Heat-Generating
- Weight Saving
- Miniaturization, High-Density
- High Efficiency

Miniaturization and High-Density involves many technology
5μm (5000nm) @ 1977 $\Rightarrow$ 1μm (1000nm) $\Rightarrow$ 500nm $\Rightarrow$ 130nm @ 2011
3. Evolution of the technical elements

Packaging: IC, Passive Device, Electric Parts, Printed Board

<table>
<thead>
<tr>
<th>Year</th>
<th>Miniaturization, Lightweight</th>
<th>Thinner, Multiple functions</th>
<th>Smartphone, Large screen</th>
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</thead>
<tbody>
<tr>
<td>'90</td>
<td>QFP</td>
<td>Tape Carrier Package</td>
<td>Package on Package</td>
</tr>
<tr>
<td></td>
<td>0.5mm Pitch</td>
<td>1.2mm Pitch</td>
<td></td>
</tr>
<tr>
<td>'00</td>
<td>TCP</td>
<td>BGA</td>
<td></td>
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<tr>
<td></td>
<td>1.0mm x 0.5mm</td>
<td>0.6mm x 0.3mm</td>
<td></td>
</tr>
<tr>
<td>'10</td>
<td>BGA</td>
<td>BGA</td>
<td>Pa-PVBGA</td>
</tr>
<tr>
<td></td>
<td>0.4mm x 0.2mm</td>
<td>0.4mm x 0.2mm</td>
<td></td>
</tr>
</tbody>
</table>

- **<IC>**
  - QFP 0.5mm Pitch
  - TCP 1.2mm Pitch
  - BGA 0.6mm x 0.3mm
  - BGA 0.4mm x 0.2mm
  - Pa-PVBGA 0.4mm x 0.2mm

- **<Passive Device>**
  - 1.6mm x 0.8mm
  - 1.0mm x 0.5mm
  - 0.6mm x 0.3mm
  - 0.4mm x 0.2mm

- **<Printed Board>**
  - Any Layer (Plated Via)
  - Rigid FPC
  - Build Up
  - Embedded components
  - S Layer 100um / 100um
  - 10 Layer 75um / 75um
  - 12 Layer 50um / 50um
  - 10 Layer 40um / 40um

Ratio of '20
- *8.3*
- *1/64*
- *7.8*
Parts level

1. Mixed signal SOI-ASIC (1/2)

Status: Element evaluation

- Concept for the System On Chip
- ADC, DAC, Analog Multiplexer, Regulator, PWM with domestic technology
- SOI technology for radiation-hardened and low-power consumption
- NOW: ADC sample testing
- By 1st Q 2016: QT sample will be prepared
Parts level

Infusion of New Technology into MIL Standards
Adding Class Y to Microcircuits Specification

- Microcircuits specification, MIL-PRF-38535
  - Revision K was released December 20, 2013
  - Introduces Class Y

- Acknowledgements
  - Special thanks to DLA-VA
  - Thanks to everyone including task group (TG) members and advisors

- Class Y Status
  - See the next sheet

Class Y – Non-Hermetic ICs for Space

- Why insert Non-Hermetic ICs into space systems?
  - Advancements in packaging technology, increasing functional density, and increasing operating frequency have resulted in single die SoCs with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - There was a desire for the performance and without industry coordination, each OEM would be attempting to qualify the devices on their own – and having to convince their customers the qual was adequate

- Challenges
  - Deciding which non-hermetic technologies to focus on
  - Focusing on technology issues specific to non-hermetic and not technologies that happen to be used in a non-hermetic device under consideration (such as flip chip, BGA, or new underfills)
    - But still starting other activities to address these technologies
Parts level

Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance

Task Group Activities
- Review M. Sampson idea
- Class Y Concept Development
- EP Study (DLA-VA)
- Coordination Meeting at DLA Land & Maritime (April 2012)
- DLA-VA to update 38535 with Class Y requirements and release the draft version (rev. K) for comments
- DLA-VA to begin preparation for auditing Class Y suppliers
- 38535K Coordination Meeting
- DLA-VA to date 38535K
- DLA-VA to begin audit of suppliers to Class Y requirements
- Manufacturer Certification to QML-Y (DLA-VA)
- Users to procure QML-Y flight parts from certified/qualified suppliers

Task Group Inputs
- Government
- Manufacturers
- Primes
- Others

G-12 Class Y Task Group Non-Hermetics in Space

- Aerotek (October 2011)
- Xilinx February 2012
- Honeywell (May 2012)
- BAE (October 2012)
- e2v January 2013
- Supplier PTDT** Presentation
- CWSE Feb. 2013, LA Conference

Newly Formed Task Groups with Class Y Interest
- J-13.2 Electronic Parameters B. B1.1/Standardization
- J-13.2 PRCCHIP Package BFA RD G4A** Requirements
- J-13/4/12 B-11 BMEs (base metal electrodes)

Other Task Groups with Class Y Interest
- J-12 Plastics Subcommittee
- J-13.2 500A6 Testing BFA/RDA
- J-13 TJ requirements

**PTDT = Package Integrity Demonstration Test Plan
**BFA = CDA = bi-axial array/collimated array

NASA
Parts level

Identified Key Technologies for ESA (EEE 2020 Roadmap)

- Space qualified supply chain for 65nm Deep SubMicron ASIC technology. ADC/DAQ HSSL, Flip-chip, DDR memories, high pin count packaging
- Rad hard Large re-programmable European FPGA.
- European space qualified Gallium Nitride (GaN) supply chain for POWER and RF.
- Space qualification of Non Hermetic packaged devices (e.g. Class V)
- Space qualification of European Mixed Signal ASIC technology.
- Extended range of advanced VLSI products:
  - DC-DC Converters, MOSFETS, Pulse Width Modulators, Line driver etc...
- Next Generation general purpose Micro-Processor (NGMP)
- European high performance CMOS image sensor technology supply chain
- Space qualified European RF MEMS process.
- Qualification of non-European foundry processes (Far-East foundries)
- Process re-qualification due to REACH/RoHs induced changes
- Evaluation of Commercial EEE Components for Space applications.

Risk assessment of HV Silicon and SiC diodes (2)

Why use SiC Diodes (2)?

- Schottky diode
  - No reverse recovery losses  
    => Lower power losses!
- Wider band-gap (3.23 eV) compared to (<2V) for Si  
  => Higher breakdown electric field strength
- Very often “inherent radiation hardness” is advertised!
Parts level

65 nm Rad-Hard Platform Status

- 4 Running ASIC & ASSP Developments
  - ST partnering with ATMEL on some European projects
    - CNES and ESA Funded programs
    - 1st Tape out 4Q14/1Q15 can be used for 1st Qualification Domain
  - ST frontline on some other European projects
    - ESA Funded Program – Tape out
- Packaging: In development
  - Wire Bonding & Flip Chip Solutions
- Additional Test Chip: Under Evaluation
  - Includes New Digital IPs: Serdes, Fast Flip-Flop
  - Electrical Test: 4Q14 - Radiation Test: 1Q15
- First ESCC Qualification: 2015

RT FPGAs Migrating to High Speed Processing

Ready for Design
Parts level

Evaluating Automotive Electronic Parts

- The main drivers are size, weight, and price of electronic components
  - Commercial electronic parts usually offer varied functions
  - How do automotive parts compare to catalog commercial?

- Commercial Parts Options
  - Manufacturers make parts to meet the needs of their chosen market(s)
  - Automotive parts are designed to meet the needs of sub-system suppliers to automobile manufacturers

- Space
  - Parts from manufacturers that are qualified to the ACEG seem to offer advantages for the smallsat user
  - NASA is doing a limited evaluation of automotive electronics

PEMS Approach

Review phases
I: Baseline review for screening and comparison
II: Baseline review for qualification and comparison
III: Review for any enhancement or changes
IV: Critical process control review
V: Final recommendations

Comparison of known Industry PEMs Row and Major SubsiOEM

Commonality and consensus was to use Marshall MSFC-STD-3012 as baseline
Assembly level

Package mounting (Technical issues)

- Vibration and mechanical-shock tolerability
- Thermal-shock tolerability (Relief of the heat stress which occurs due to the CTE mis-match)

Fig-9: a mounting sample of a package on a PCB

Fig-10: a sketch of mounting portion and the heat stress

1. Miniaturization and High-Density Technologies of PCB
Assembly level

4. Summary report of miniaturized PCB

- Improvement of placement accuracy of a component mounter

Reduction of placement gap from 0.2 mm to 0.08 mm between parts
Realization by continuing to maintain the limit of a mounter

Pb-free

- Why insert Pb-free into military and space systems?
  - Legislation in EU and Asia led to many commercial parts and units converting to Pb-free solders and finishes
  - While most have exempted or excluded military, avionics, and space products, many suppliers are converting their lines to Pb-free due to "dual use"

- Challenges
  - The most common Pb-free finish is tin (Sn) which can form whisker
    - Creates shorts, debris, and possibly plasma events (in space)
  - Pb-free solders for attach do not have the history and reliability data of SnPb
  - Qualification for SnPb attach may not be applicable for Pb-free because the acceleration models are different
Assembly level

3. Evolution of the technical elements

- Component embedded PCB

Features:
- About 250 passive components are embedded to achieve a 15% board miniaturization compared to conventional models.
- Solder reflow connection.
- Stress reduction in the heat dissipation of parts by the resist coating.

Example of High Density Mounting

Murata’s High Density Mounting Technology
- Ultra Small Sized MLCC (0201, 01005, 008004)
- Ultra Low Profile MLCC (Thickness: 220um~)
- High Capacitance MLCC (100uF~)
- Embedded Capacitor (0402, 0201)
- Low ESL Capacitor (Three Terminal, Reverse Geometry Capacitor)
Assembly level

Multi-Chip Modules (MCM)
- Multiple discrete components in a single package to reduce footprint.
- Hybrid may remove need to external passives
- Simplify board design

Example: Honeywell 64Mb MRAM
- Next generation from GMLV qualified 16Mb MRAM to 64Mb MRAM
- Dramatic reduction in space:
  - 16Mb package 28.5mm x 28.5mm
  - 64Mb MCM package 42.7mm x 42.7mm
- MCM technology to create a larger FPGA, high applications
- Successful demonstration of Honeywell device for Xilinx Virtex FPGA

Key specifications:
- Radiation hardened: >1M Rad TID
- Magnetically shielded Ceramic package
- Reliability > 10 years
- Endurance: unlimited write endurance
- -40°C to +125°C Temp Range

E2V Flip Chip Assembly
- Flip chip production started in 2000 at e2v Grimsby
- Production line has been upgraded in 2005
- More than 100k manufactured in military levels
- 32 Channel Multiplexer Concept Design

- WLCSP dimensions and features
  - 5000um x 4800um module size
  - 9 x 7 ball grid array with 0.5mm pitch
  - 3 dummy bumps in corners
  - Improves board level reliability i.e. shock and vibration
- No grid array in center of package
- Each PGB Lagmatix
- Reduces FCB cost and increases reliability
  - No vias under pad or blind and buried vias
- Board area saving compared to a packaged device
  - Do not forget to include the leads or solder pad openings
New Technology

Wireless Energy Transmission and Harvesting

The Wireless Sensor System in a Spacecraft and a Rocket

- Realization of safe transportation for a spacecraft and a rocket by a wireless sensor network system.

- Battery-less health monitoring sensors with microwave power transmission and energy harvest spacecraft.

Wireless Energy Transfer and Harvesting

The WiSEnT in a Rocket

RVT

Inner Field Test

Institute of Space and Astronautical Science

Kawasaki Research Laboratory
Challenge

Monolithic vs. Hybrid Microcircuits and Related Issues

- **Standard Microcircuits**
  - Monolithic
  - Hybrid

- **# Elements**
  - Single
  - Multiple

- **MIL Spec**
  - MIL-PRF-38555
  - MIL-PRF-38554

Changes in Last Few Years: The boundary between monolithic and hybrid has become blurred.

- **Capacitors Inside C Packages**
  - Single
  - Hybrid

- **Issues:**
  - Signal integrity: capacitors used in C packages
  - Outgassing
  - MIL-PRF-38555
  - MIL-PRF-38554

- **Mitigation:**
  - Added capacitor screening requirements in MIL-PRF-38555 Spec (Para 3.15)
  - Encouraging suppliers to obtain MIL-PRF-38555 Certification

A New Issue: No MIL capacitors to satisfy the needs of new high-speed, low voltage designs. They are using Commercial EME (Electro-Metal Electrode) capacitors with unproven space heritage. This affects Class V.

- **EME Used?**
  - Yes, but not tested to 3.15
  - Yes, but meet existing element evaluation requirements which are not stringent for MIL-PRF-38555

- **Mitigation**
  - Evaluate EME
    - NASA Aerospace, Suppliers, ESA, JAVA
    - Double Derating
  - Stop use until evaluation done
    - (Ref. G-12 letter to DLA)
Challenge

Infusion of New Technology into MIL Standards
Class Y
Qualifying New Packaging Technology

- Issue
  - How to address the manufacturability, test, quality, and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications?

- Change in Paradigm
  - Move away from rigid requirements; provide flexibility to manufacturers.

- Proposal
  - Each manufacturer shall develop a Package Integrity Demonstration Test Plan (PIDTP) that shall be approved by the qualifying activity after consultation with the space community. Ref: MIL-PRF-38535K, Para B.3.11.
Thank you very much & See you next MEWS!