SILICON SPACE TECHNOLOGY (SST)

JAXA MICROELECTRONICS WORKSHOP

A 130nm RADIATION HARDENED ARM® CORTEX® M0 MICROPROCESSOR

OCTOBER 2014
AGENDA

COMPANY INTRODUCTION

M0 PRODUCT SPECIFICATIONS

M0 RADIATION AND HI TEMP DATA

FUTURE PRODUCTS

SUMMARY
Provider of Ruggedized Computing Solutions and Foundational CMOS technology for
1. Extreme (150°C -> 250°C) Industrial Temperatures
2. High (50 KRad -> 300 KRad) Radiation Environments

Key Facts
• Founded in 2004; Austin, TX
• Management and key engineers have a combined 200+ years experience in the Semiconductor IC industry
• *HardSIL™* is the Foundational CMOS technology
  - Enhances standard CMOS for High Temperature and Radiation
  - Proven at GLOBALFOUNDRIES and Texas Instruments
  - Applicable to every CMOS process node, including 28nm and 16nm
  - 10 Patents issued
• Product Portfolio
  - 8M and 16M SRAMs available now.
  - ARM® Cortex® -M0 and 18M, 36M and DDR2 SRAMs available in 2015
HardSIL™ and Product Development Timeline

- 40 nm @ GLOBALFOUNDRIES
- Mixed Signal @ GLOBALFOUNDRIES (130 nm)
- SRAM & Cortex-M0 @ GLOBALFOUNDRIES (130 nm)
- SRAM @ Texas Instruments (180 & 130 nm)
- HardSIL™ Development (Independent of Foundry or Process Node)

Process Migration
Test Vehicle
JEDEC Qualified SRAMs
Digital Integration with ARM Cortex-M0

6 SBIR Funding Contracts
16M SRAM QML-V Qualified for radiation

Years: 2004 to 2015
Technology and Solutions

Ruggedized Computing Solutions

Wafers / Bare Die

Components

Single Board Computers

HardSIL™ Foundational CMOS Technology

HardSIL™ Silicon IP
HardSIL™ Cell Library & I/O
HardSIL™ Circuit Models
HardSIL™ Layout Rules
HardSIL™ SP, DP SRAM
HardSIL™ Efuse, POR, PLL

HardSIL™ ASIC
HardSIL™ ARM Cortex-M0
HardSIL™ Memory
HardSIL™ IP Blocks
HardSIL™ Mixed Signal

Commercial Foundry

High Reliability Products
- High Temperature
- Radiation Hardened

SST Inc. Confidential
HardSIL™ devices serve Radiation Effects markets

- 300 KRad hardness.
- Latch up immune.
- Temperature range from -55°C to +125°C.
- Extends satellite life time

16M SRAM sold into multiple Satellite applications
**HardSIL™ devices serve High Temperature markets**

- **HardSIL™** enables IC operating temperature to 250°C.
- **HardSIL™** is Latch up immune at >250°C.
- **HardSIL™** increases IC lifetime at Temp > 200°C.
- **HardSIL™** offers a platform solution for all IC’s required for DHD signal chain at temperatures > 200°C.
- **HardSIL™ at 130nm** offers opportunity to integrate FPGA functionality with microprocessor and DSP.

**18M SRAM demonstrated @ 250°C over 350 hours**

**ARM Cortex-M0 demonstrated @ 250°C**
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SUMMARY
ARM® Cortex®-M0
Embedded System Controller

► Specifications
- CPU: 50 MHz ARM® Cortex®-M0 (worst case)
- Process: 130nm, 1.5V Core Voltage
- Package: 188 CQFP

► Key Features and Advantages
- Latch up Immune with HardSIL™ Hardened by Process Technology on Standard CMOS
- 16KB Data and 16KB Program Memory with ECC
- 32 Counter/Timers with Extensive Hardware/Software Triggering
- 2 SPI and 2 UART External Interfaces
- 32 Dedicated General Purpose 3.3V I/O (GPIO)
- Memory Controller for Hardened SST Synchronous Burst Memory (2M x 36)

► Key Radiation Hardened Features
- Triple Mode Redundancy (TMR) / DICE Registers
- Optional Scrub Engine on Memories to Eliminate Error Accumulation
- Hardened Boot Controller with ECC
ARM® Cortex®-M0 (Rev 2) Embedded System Controller

Specifications
- **CPU**: 50 MHz ARM® Cortex®-M0 (worst case)
- **Process**: 130nm, 1.5V Core Voltage
- **Package**: 64 CQFP

Key Features and Advantages
- Latch up Immune with HardSIL™ Hardened by Process Technology on Standard CMOS
- Power Gating and Hardware Debugger
- 32KB Data and 128KB Program Memory
- 24 Counter/Timers with Extensive Hardware/Software Triggering
- 2 SPI, 2 I²C, and 2 UART External Interfaces
- 40 Multiplexed General Purpose 3.3V I/O (GPIO)

Key Radiation Hardened Features
- Triple Mode Redundancy (TMR) / DICE Registers
- Optional Scrub Engine on Memories to Eliminate Error Accumulation
- Hardened Boot Controller with ECC

System Control
- JTAG
- Power on Reset
- Clock & Reset
- 24 Counter/Timers Extensive Triggers
- Watch Dog

Internal Memory
- 32 KB Data
- 128 KB Program

CPU Platform
- ARM Cortex-M0
- Triple Mode Redundancy (TMR) Registers(RH)
- Majority Voting and Update

AHB Lite / APB Bus Interface

Connectivity
- UART x2, 2Mbps
- SPI x2
- I²C x2
- 3.3V Mux GPIO (Max 40)
Software Environment – Debug

User Interface GUI

Software Emulation

Peripheral Simulation Models for M0

Hardware Operation

Before Development Board and components are available, use Keil emulator to model board functionality
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FUTURE PRODUCTS

SUMMARY
HardSIL™ SEU Avoidance Techniques:

- Libraries
  - Buried Guard Ring (BGR)
  - Dual Interlocking Storage Cells (DICE)
  - Triple Mode Redundancy (TMR)
  - Registers
  - Logic
  - Gated clock with TMR refresh

- Memories:
  - Error Detection And Correction (EDAC)
  - Write-back
  - Scrub
  - Bit-cell physical separation

- Electronic Design Automation (EDA):
  - TMR register insertion
  - TMR logic insertion
  - In-line register placement avoidance

- Design:
  - Glitch filtering on critical signals
  - Configuration control through IOs
  - Boot loaders with Cyclic Redundancy Check (CRC) Checking/reloading
RADIATION DATA - TID:

HardSIL™ SRAM typical standby current vs TID

SST Inc. Confidential
RADIATION DATA - SEE:

**Weibull plot for bit error cross-section (cm²/bit) vs effective LET (MeV-cm²/mg)**

for typical HardSIL™ SRAM

Below the diagram:

`<-- 1E-14 w/ scrub`
Radiation Data Summary:

• Total ionizing dose performance without functional errors and with well-controlled typical post-radiation currents:
  • At 650Krad(Si) and 25°C the typical post-rad standby current is < 2mA.
  • At 300Krad(Si) and 25°C the typical post-rad standby current is < 400uA.

• Effective elimination of uncorrectable word errors regardless of ion LET and angle of incidence when Scrub frequency is chosen to prevent accumulation of native errors in the array.

• The SER rate with EDAC and Scrub frequency of 111KHz is calculated at less than $5 \times 10^{-14}$ errors/bit-day (at geosynchronous orbit, solar minimum).

• The HardSIL™ process provides single event latchup immunity for any LET at any angle, as is confirmed up to 150°C while operating at 110% of core voltage, and LET > 117 MeV-cm$^2$/mg.

• A typical dose-rate threshold of $\sim 8 \times 10^9$Rad(Si)/s
• A dose-rate survivability $> 1.7 \times 10^{11}$Rad(Si)/s
Lab Board Temperature Tests

- **Lab Board**
- Temperature controlled by Omega controller
- Thermocouple placed on top of device
- Heater placed under device in socket
ARM® Cortex®-M0
Dhrystone IDDcore vs. Clock Frequency

PA32KASA Dhrystone IDDcore By Clock Frequency, Temperature

Temperature
- 55
- 85
- 125
- 150
- 175
- 200
- 220
- 230
- 240
- 250
- 260

IDDcore @ VDDcore = 1.5V (A)

Clk (MHz)
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FUTURE PRODUCTS

SUMMARY
ARM Cortex-M4
Embedded System Processor with DSP Engine

Specifications
- CPU: 80MHz ARM Cortex-M4
- Process: 130nm, 1.5V Core Voltage
- Package: 128 CQFP

Key Features and Advantages
- Latch up Immune with HardSil™ Hardened by Process Technology on Standard CMOS
- Power Control and Hardware Debugger
- 32KB Data and 128KB Program Memory with ECC
- 32 Counter/Timers with Extensive Hardware/Software Triggering
- 2 SPI, 2 I²C, and 2 UART External Interfaces
- 40 Multiplexed General Purpose 3.3V I/O (GPIO)

Key Radiation Hardened Features
- Triple Mode Redundancy (TMR) Registers
- Optional Scrub Engine on Memories to Eliminate Error Accumulation
- Hardened Boot Controller with ECC
- Memory Controller for Hardened SST Synchronous Burst Memory (2M x 18)
Digital and Mixed-Signal Integration

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<td>ARM® Cortex™-A5 Up to 266 MHz</td>
<td>12-bit ADC x2</td>
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<td>12-bit DAC x2</td>
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<td>FlexTimer (2-ch.)</td>
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<td>SAI x3</td>
<td>Secure JTAG</td>
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<td>ESI</td>
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CMOS enables integration of this magnitude

*HardSIL™* enables CMOS to operate in extreme environments

NOTE: Publicly available image at Freescale.com
SUMMARY

*HardSIL™* foundational CMOS technology:

- Enhances a “Hardened by Design” IC with a “Hardened Process”.
- ProvidesLatch up immunity.
- Withstands 300 KRad Total Ionizing Dose (TID)
- Enables IC operating temperatures from cryogenic to +250°C.
- Increases IC operational lifetime at *every* temperature.

**Ruggedized Computing Solutions:**

- Broad family of SRAM products
- ARM processors specifically designed for the Radiation and High Temperature markets
THANK YOU

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