Aeroflex Non-Volatile and Volatile Memory Solutions

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Aeroflex Qualified Memory Solutions

- Aeroflex Colorado Springs has been committed to memory solutions for over 20 years
- Quality Tradition built on PROM and SRAM
- Industry Leader in High Density Stacking and MRAM Technologies
- QML Qualified QCOTs
  - SDRAM
  - NOR Flash

Aeroflex HiRel Memory Solutions

SSRAMs
- 64M to 96M
- 32bit to 48bit
- bus width
- Built in EDAC

DRAMs
- SDRAM
- 2.5G & 3.0G
- 40bit and 48bit
- bus width

Non Volatile
- MRAM
- 16M & 64M
- NOR-Flash
- 64M
Synchronous SRAMs (SSRAMs) Join Memory Family

**Volatile Memories**

**SSRAMs 64M, 80M, 96Megabit:**
- UT8SP2M32/40/48 with Continuous Data Transfer (CDT) architecture, Pipelined, 2 clock cycle latency, 7.2Gbps
- UT8SF2M32/40/48 CDT, Flow-thru, 1 clock cycle latency, 3.98Gbps

**SRAMs 4M up to 160Megabit:**
- UT8Q512E: 4M, 512K x 8bit, 3.3V, 50MHz, 400Mbps
- UT9Q512E: 4M, 512K x 8bit, 5V, 50MHz, 400Mbps
- UT8Q512K32E: 16M, 512K x 32bit, 3.3V, 40MHz, 1.28Gbps
- UT9Q512K32E: 16M, 512K x 32bit, 5V, 40MHz, 1.28Gbps
- UT8R128K32: 4M, 128K x 32bit, 3.3V I/O, 66MHz, 2.1Gbps
- UT8R512K8: 4M, 512K x 8bit, 3.3V I/O, 66MHz, 528Mbps
- UT8ER512K32: 16M, 512K x 32bit, 3.3V I/O, 50MHz, EDAC, 1.6Gbps
- UT8ER1M/2M/4M32: 32, 64, 128M, 1M, 2M & 4M x 32bit, 2.5V & 3.3V I/O, 50MHz, EDAC, 1.6Gbps
- UT8ER1M/2M/4M39: 40, 80, 160M, 1M, 2M & 4M x 39bit, 2.5V & 3.3V I/O, 50MHz, 1.95Gbps

**SDRams 2.5G and 3.0Gbit:**
- UT8SDMQ64M40: 2.5G, 64M x 40bit, 3.3V I/O, 100MHz, 4Gbps
- UT8SDMQ64M48: 3.0G, 64M x 48bit, 3.3V I/O, 100MHz, 4.8Gbps

**Non-Volatile Memories**

**MRAMs 16M and 64Mbit:**
- UT8MR2M8: 16M, 2M x 8bit, 3.3V I/O, 25MHz
- UT8MR8M8: 64M, 16M x 8bit, 3.3V I/O, 20MHz

**NOR Flash 64Mbit:**
- UT8QNF8M8: 64M, 8M x 8bits, 3.3V I/O, 16.6MHz reads

**PROMs 256Kbit:**
- UT28F256QLE: 256K, 32K x 8, 5V, 22.2MHz reads
- UT28F256LVQLE: 256K, 32K x 8, 3.3V, 15.3MHz reads
SSRAM Product Description

▼ 64, 80 & 96Mb SSRAMs with Continuous Data Transfer (CDT)
– Pipelined architecture delivers 40-150MHz 100% bus efficient operation
  ▼ Inputs and outputs registered with two clock cycle latency
– Flow-thru architecture delivers 40-83MHz 100% bus efficient operation
  ▼ Inputs registered with single clock cycle latency
– CDT eliminates wait states between read and write operations
– Three Chip Enables (/CS0, CS1, /CS2) for simple depth expansion
– Clock Enable (/CEN) to enable or suspend clock
– Synchronous self-timed writes with asynchronous output enable
– Four word burst capability - interleaved or linear
– Single 2.5V or 3.3V supply (14mW/MHz & 18mW/MHz respectively)
– “ZZ” and “SHUTDOWN” mode power saving options
  ▼ 20% and 80% reduction respectively
– Multiple bus width options for design flexibility
  ▼ 2M x 32 (with embedded autonomous EDAC)
  ▼ 2M x 40 (8 additional bits for external EDAC)
  ▼ 2M x 48 (16 additional bits for external EDAC)
– High density in monolithic silicon: ≤ 12pf typical load lead capacitance
– Package in 288-lead CLGA (ceramic land grid array) & CCGA (column grid array)
SSRAM CDT (Continuous Data Transfer)

- **Continuous Data Transfer**
  - Data transfers on every clock cycle
    - **Pipelining**
      - The practice of capturing commands, addresses, and data information in order perform multiple instructions simultaneously.
    - **Latency**
      - The amount of time an instruction requires to complete. The typical read access latency, for example, of the SSRAM is ~ 9ns
    - **Clock Cycle Latency**
      - The number of complete clock cycles that transpire during the latency time
  - Read or write commands are sequentially interchangeable without encountering any latency penalty

- **Full Random Access**
  - SSRAM’s internal architecture performs all necessary function in the background for random access, data coherency, and error correction simplifying interface similar to SRAM
  - Typical DRAM multiplexes address bus resulting in row and column access latencies
SSRAM CDT Design Strengths

- **Aeroflex Continuous Data Transfer (CDT)**
  - Equivalent with high performance ZBT™, NoBL™, and No/Zero wait state memories
  - Applications requiring frequent bus turnaround
    - Achieved through write data realignment where address-to-data relationship is identical for both read and write accesses
  - Applications requiring random access
    - No latency penalty for continuous access to any location
  - Applications requiring low latency
    - Flow-thru: 100% bus efficiency after initial one clock cycle latency up to 83MHz
    - Pipelined: 100% bus efficiency after initial two clock cycle latency up to 150MHz
  - Applications for:
    - Fast buffer and look up table access
      - Image processing
      - Peripheral instrumentation
      - Network data streaming (switches and routers)
      - Robotic control systems
      - Algorithmic computations
    - Level 2 (L2) Cache
      - Mainframes, PCs, RISC, FPGAs, and DSP system
    - Faster configuration data access for slower non-volatile data

Prototypes and IBIS Models Available Now!
What Applications Match SSRAM?

- Sun/Star Sensor Maps
- Electro-optical Imager Conversion Tables
- Sensor Look-Up Tables
- Sensor Calibration File
- Linked Lists
- Routing Look-Up Tables
- Antenna Array Calibration Files
- Processor Instruction Caching
- NV-Memory Buffering
Value Proposition for Aeroflex SSRAM

▼ Why Aeroflex Synchronous SRAM
   – Proven track record
     ▼ Superior Radiation Performance – via Design & Process Techniques
     ▼ Aeroflex Colorado Springs providing quality memory solutions for over 20 years while additionally providing superior customer support
     ▼ Established Quality and Reliability
     ▼ Industry Leader in High Density Stacking
     ▼ Assured, Long Term Supplier
     ▼ DLA Approved Source QML Q and V
   – Burst mode is a high speed method to access SRAM with lower address bus noise
     ▼ Reduced activity on address bus
     ▼ Address generation to SRAM which allows controller to perform other functions
     ▼ Increased reliability due to address location generates from inside the SRAM
   – Ideal in buffering applications where
     ▼ Random access are prevalent
     ▼ Low latency and moderate density is required
     ▼ Data integrity of highly available memory is critical (Embedded EDAC)
   – Versatile architecture with various densities and both pipeline and flow-thru options
High Density SDRAMs - QCOTS

- 2.5Gb - configured as 64M x 40 (using 5 (64M x8 die) SDRAM die)
  - Optimally interfaced to 32 bit data bus with hamming code EDAC
  - Perfect for interfacing to UT699!
- 3.0Gb – configured as 64Mx 48 (using 6 (64M x8 die) SDRAM die)
  - Optimally interfaced to 32 bit data bus with Reed-Solomon EDAC
- TID of 100 krads(Si) and SEL immunity of 111MeV-cm²/mg
- 100MHz maximum frequency
- 128 CQFP, shallow side-braze and deep side-braze
- Hi-Rel temperature range: -40°C to 105°C
- Perfect for interfacing to UT700 & GR712
Aeroflex Qualified Non-Volatile Solutions

**QCOTs NOR Flash**
- Fast 60ns read access
- Simultaneous read/write operations
- 10 & 50 krads(Si)
- 64Mb
  - Byte or Word Configurable (8Mx8bits or 4Mx16bits)

**MRAM Technology**
- Licensed from Everspin
  - Proven Commercial Process
- Fast 45ns write read access
- Symmetrical read/write cycles
- 100 krads(Si) to 1 Mrads(Si)
- 16Mb & 64Mb Options
  - Bus widths x 8bits
# 64 Megabit Non-Volatile NOR Flash

## Features

- Configurable in Byte mode 8M x 8bit or Word mode 4M x 16bit
- 60ns read access time
- 7us/word programming time
- Cycle endurance: 10K cycles per sector
- Data retention: > 20 years @ +90°C
- Single 3.3V power supply
- Ultra low typical power consumption
  - 4mA active read current at 1MHz
  - 16mA active read current at 5MHz
- Simultaneous read/write operation
- Flexible bank architecture
- JEDEC pinout and software compatible with single-power-supply flash standard
- Supports Common Flash Memory Interface (CFI)
- CMOS compatible
- HiRel Temperature range (-40°C to 105°C)
- 48 pin ceramic Flatpack
- Operational environment
  - Total dose: 10 or 50 krad(Si)
  - SEL Immune: 80 MeV-cm²/mg @ 85°C
  - SEU Immune: Memory Cell 100MeV-cm²/mg @ 25°C

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QML Q & Q+ Qualified!

IBIS Models Available Now!
16 Megabit Non-Volatile MRAM

▼ Features

– Organized as 2M x 8bit bus
– Single 3.3V Power Supply
– Fast 45ns read/write access time
– Functionally compatible with traditional asynchronous SRAMs
– HiRel Temperature range (-40°C to 105°C)
– Automatic data protection with low-voltage circuitry to prevent writes on power loss
– CMOS and TTL compatible
– Data non-volatile for > 20 years at temperature
– Read/write endurance: Unlimited for 20 years
– Two 40 pin ceramic flat-pack options available
  ▼ 50 mil pin pitch (.8” x 1.22”)
  ▼ 25 mil pin pitch (.8” x .95”)

– Operational Environment
  ▼ Total dose: TID: 100k, 300k, 500k, & 1 Mrad(Si)
  ▼ SEL Immune: 100 MeV-cm²/mg @ 105°C
  ▼ SEU Immune: Memory Cell 100 MeV-cm²/mg @ 25°C
– Standard Microelectronics Drawing (SMD)
  ▼ QML Q and Q+ Qualified
  ▼ V Pending

Magnetic Field Specs:
8000 Å /m or ~ 100 G for reads, writes, & standby

QML Q and Q+ Available now!
IBIS Models Available Now!
64 Megabit Non-Volatile MRAM MCM

Features
- Organized as 8M x 8bit bus
- Single 3.3V Power Supply
- Fast 50ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- HiRel Temperature range (-40°C to 105°C)
- Automatic data protection with low-voltage circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data non-volatile for > 20 years at temperature
- Read/write endurance: Unlimited for 20 years
- 64-pin ceramic Flatpack package
- Operational environment:
  - Total dose: TID: 100k, 300k, 500k, & 1 Mrad(Si)
  - SEL Immune: 100 MeV-cm²/mg @ 105°C
  - SEU Immune: Memory Cell 100 MeV-cm²/mg @ 25°C
- Standard Microelectronics Drawing (SMD), QML Q, Q+, and V pending
- Target application: configuration memory for Xilinx XQR5V FPGAs

QML Q/Q+ Targeted for November 2014!!

Prototypes and IBIS Models Available now!

Magnetic Field Specs:
8000 Â/m or ~ 100 Oe for reads, writes, & standby
Summary

- Committed to Memory Past, Present and Future
  - Extensive History of Latch up Immune, Enhanced Operational Hardened Memories
  - Latest Products:
    - Stacked SDRAMs UT8SDMQ64M40 (2.5G) and UT8SDMQ64M48 (3G) in same universal package
    - 64Mb NOR FLASH UT8QNF8M8 - In Production
- Proven Hardening, MCM and Qualification approach
- Assured Long Term Supplier
- QML Q and Q+ 16M MRAM Available!!
- Prototyping: 64Mb Non-Volatile MRAM
  - High density monolithic; Intrinsically SEU immune; Infinite endurance; Long Term Data Retention; Fast read/write
- In Development: SSRAMs 64M, 80M, 96Megabit
  - UT8SP2M32/40/48 with Continuous Data Transfer (CDT) architecture, Pipelined, 2 clock cycle latency, 6.4Gbps
  - UT8SF2M32/40/48 CDT, Flow-thru, 1 clock cycle latency, 3.8Gbps